ADVANCES IN CYBER-PHYSICAL SYSTEMS

Vol. 1, No. 2, 2016

SATELLITE SCIENTIFIC DATA COLLECTION AND ACCUMULATION SYSTEM AS A BASIS FOR CYBER-PHYSICAL SYSTEMS CONSTRUCTION

Valerii Hlukhov[1], Adolf Lukenyuk, Sergii Shenderuk

[1]Lviv Polytechnic National University, 12, Bandera str., Lviv, 79013, Ukraine.
Lviv Centre of Institute for Space Research of National Academy
of Sciences and the State Space Agency of Ukraine, 5-A, Naukova str., Lviv, 79060, Ukraine
Authors e-mail: glukhov@polynet.lviv.ua

Submitted on 12.12.2016

© Hlukhov V., Lukenyuk A., Shenderuk S., 2016

Abstract: **The paper reviews technologies of computer systems the development of which has led to the emergence of cyber-physical systems – there are embedded computer systems, open systems interconnection model, multilayer computer systems, wireless communications, microelectro-mechanical systems, data protection technologies. It is noted that there are computer systems exist, whose parameters are close to those of cyber-physical systems ones, there are also groups of developers who have experience of in such systems designing. The satellite scientific data collection and accumulation system developed in Lviv Center of Institute for Space Research of NAS and SSA of Ukraine with the participation of Lviv Polytechnic National University Computers department is an example of such systems. In paper The main features of this system are described in the paper. The recommendations are given onf using it as the basis for the creation of advanced cyber-physical systems.**

Index Terms: **cyber-physical system, scientific data collection and accumulation system, source packet, transfer frame, FPGA, SciWay.**

I. INTRODUCTION

The emergence of cyber-physical system (CFS) concept celebrates the next stage of computer systems and networks development, when gradual quantitative changes of their characteristics once again led to a qualitative change. Embedded computer systems evolved among computer systems, microelectromechanical systems started to be used to create sensors and actuators for them, their number increased, multi-core processors and wireless communication began to be widely used, the information exchange intensity has increased, the number of computers exceeded the number of people and even more the number of specialists who design, create and serve them, a significant part of computer systems operates a significant period of time without human intervention, total energy consumption and pollution by electromagnetic and thermal radiation increased. Necessity for special approaches to design such systems occurred. Gradual computer systems characteristics change gave rise among them such that already have been designed with application of mentioned specific approach elements. Experience iIt is advisable to study, summarize and use experience put inas the basis for advanced cyber-physical systems design approach such systems development and operation experience. Scientific data collection and accumulation system that has been developed for spacecraft “Sich-2” on board use is such a system. This article is devoted to consideration ofdiscusses its features.

II. CYBER-PHYSICAL SYSTEMS CONCEPT BACKGROUND

The starting point of cyber-physical systems can be consideredis the moment of occurrence of computer systems designed to control the certain equipment. In such systems, sensors and actuators with possible connections between them and possible man involvement in these connections take on the role of peripheral devices (Fig. 1). The interaction of several such systems was based on similar principle: there was (were) another computer system (systems) in place of an object of control. Open systems interconnection model is known [1]. Open computer systems are considered based on multilayer model (Fig. 3 [15]), standard [1] describes the functionality of each layer and the relationship between them (Fig. 2). Each layer of the system consists of protocol and special-purpose parts according to [1] in hardware implementations (Fig. 4), Protocol is realized on the basis of universal microprocessor or microcontroller, a set of special-purpose processors is realized on FPGA basis [2]. Cyber-physical systems inherited layered structure (Fig. 5) of open systems with refinements and additions [3].

The emergence of MEMS technology [5] is resulted in sensors and actuators size, weight and consumption reduction, as well as their combination in resembled integrated circuit same packages with digital controllers that control them and provide links to other elements of the computer systems (Fig. 6). The emergence of MEMS increased the number of sensors and actuators and was one of the causes of large data problem [4].

The emergence and widespread introduction of wireless computer networks technology became the next turning point in cyber-physical systems prehistory (Fig. 7).

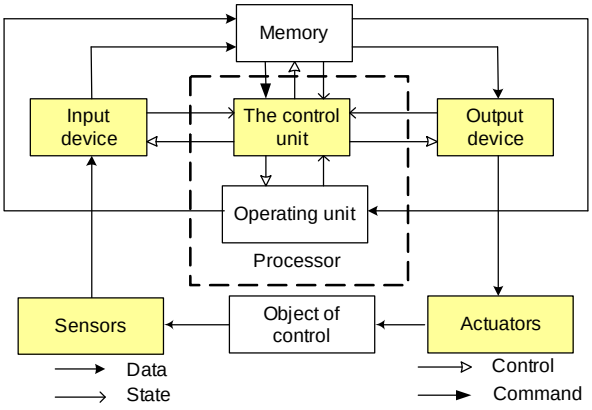

Fig. 1. Embedded computer system

The use of wireless networks sharply raised the question of information security and its credibility.

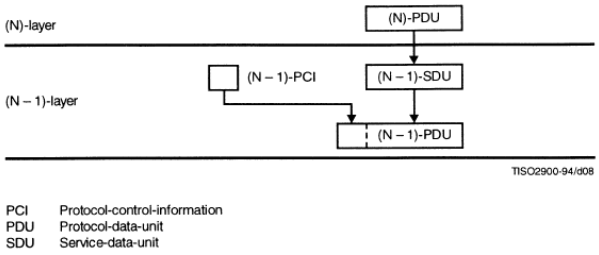

Fig. 2. An illustration of mapping between data-units in adjacent layers

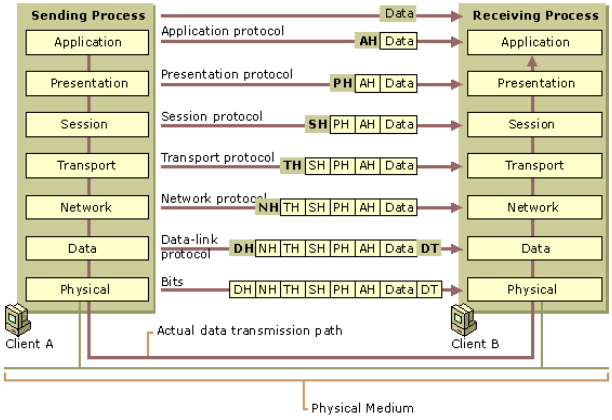

Fig. 3. Sevenlayer reference model and peer protocols (H – header, T – trailer)

III. HISTORY OF SATELLITE "SICH-2" SCIENTIFIC DATA COLLECTION AND ACCUMULATION SYSTEM

Based on the hereditary nature of cyber-physical system, to create advanced one, it is advisable to find and use a prototype, which, even without being cyber-physical system in the full sense, has its features. It is desirable that developers of future cyber-physical systems have design experience of such prototype.

"Sich-2" satellite scientific data collection and accumulation system, which was developed in the Lviv Center of Institute for Space Research of Ukrainian Academy of Sciences and State Space Agency with participation of Lviv Polytechnic National University Computers Department can pretend to be used asthe a prototype [13].

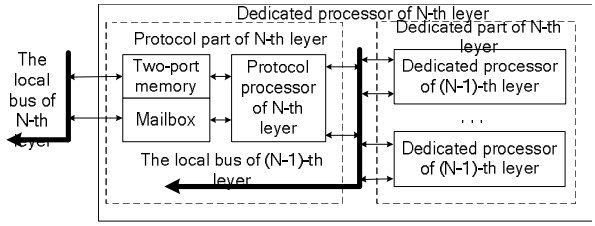

Fig. 4. The hardware implementation of the N-th layer

Scientific data collection and accumulation system from the very beginning was designed based on European Space Agency standards and recommendations [6], [7].

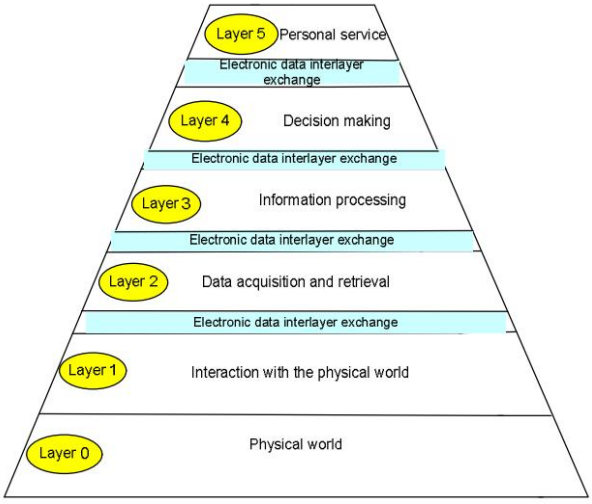

Fig. 5. CPS multilayer platform

According to these standards, system has a layered structure Fig. 8, that approaches it to cyber-physical systems. To implement the structure Fig. 8, a number of peripheral modules and the central module unit, each with the structure Fig. 4, have been developed, and together they form a multilayer structure Fig. 9 [8], which covers the structure Fig. 8.

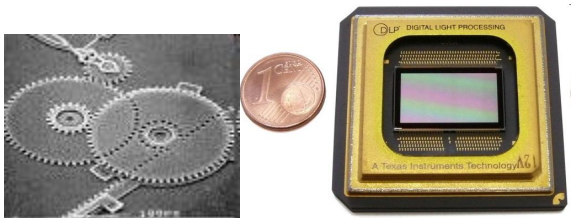

Fig. 6. MEMS

Special-purpose processors that provide variety of sensors control and are implemented on the FPGA are part as of peripheral modules as and the central unit.

Control of specific sensor is ensured by implementation in FPGA of appropriate hardware configuration, for this purpose a set of configuration files was created [10], [11], [12], [13], which is permanently updated. Software FPGA configuration is also possible by universal microcontroller (Fig. 4), that provides special-purpose processors operation modes changing.

Peripheral modules and central unit module together form a network with the help of two types of interfaces known under the titles SciWay [8]:

– high-speed interface for the exchange of scientific data at frequencies up to 250 MHz;

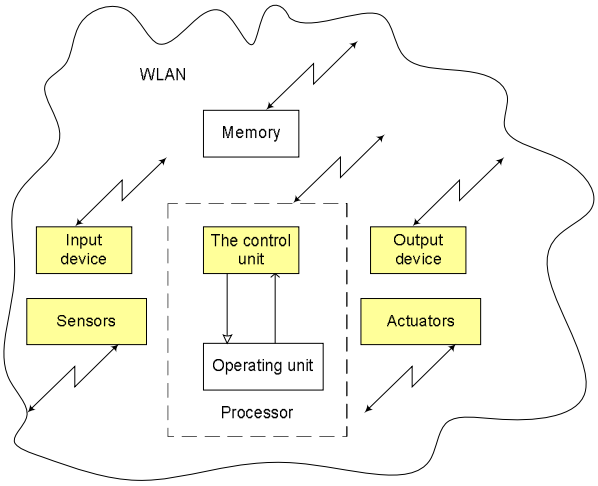

Fig. 7. WLAN

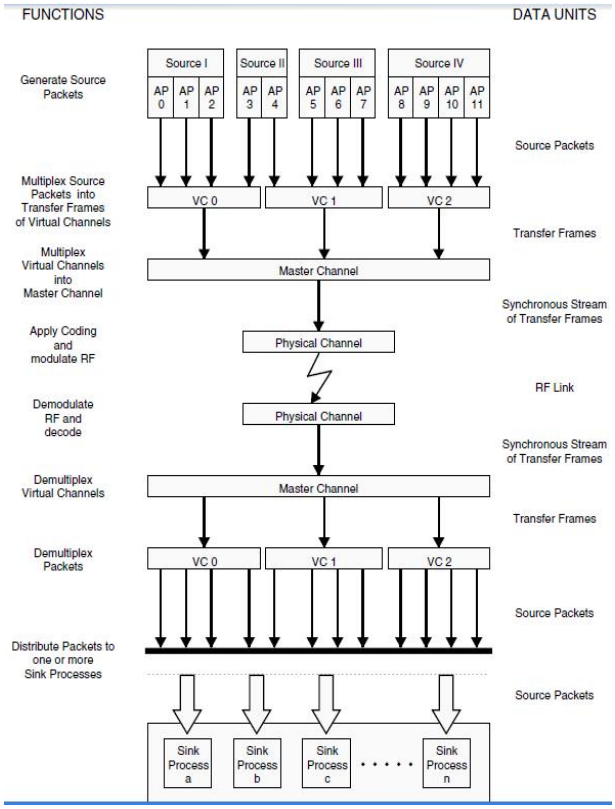

Fig. 8. ESA telemetry data transmission structure

CAN interface for commands transitions on frequency up to 20 MHz.

IV. FEATURES OF SCIENTIFIC DATA COLLECTION AND ACCUMULATION SYSTEM FOR ADVANCED "SICH" SATELLITES

Special-purpose reconfigurable scientific data collection and accumulation system is implemented on FPGA set – FPGA of peripheral module and FPGA of central unit. They are running under control of universal protocol microcontrollers. The appearance of peripheral module is shown in Fig. 11. Its basic version FPGA functional diagram is presented in Fig. 10.

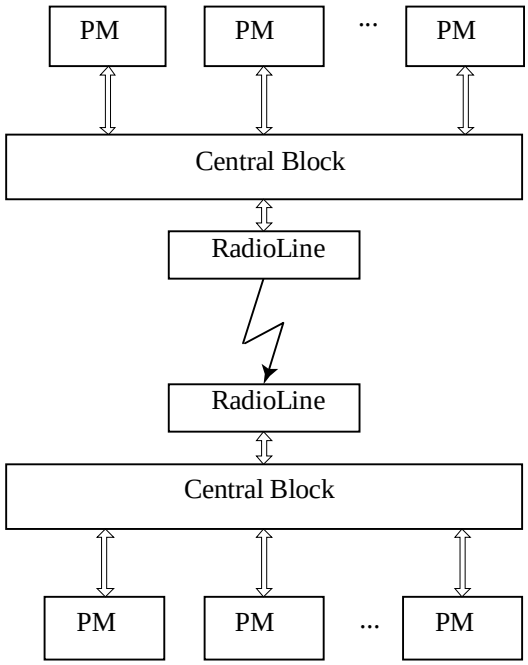

Fig. 9. Multilayer structure of scientific data collection and accumulation system (PM – peripheral module)

The basic version of the peripheral module is used as a starter kit for creation and debugging of:

peripheral modules for particular types of sensors and actuators;

sensors simulators for scientific data collection and accumulation system models;

a central unit creation. In this case, the basic version may include units that are not used in the peripheral modules.

The main function of special-purpose peripheral modules of scientific data collection and accumulation system is receiving data from various types of sensors and transfering them to the central module by unified SciWay interface. The peripheral module can also play the role of scientific data sensor simulator during scientific data collection and accumulation system debugging.

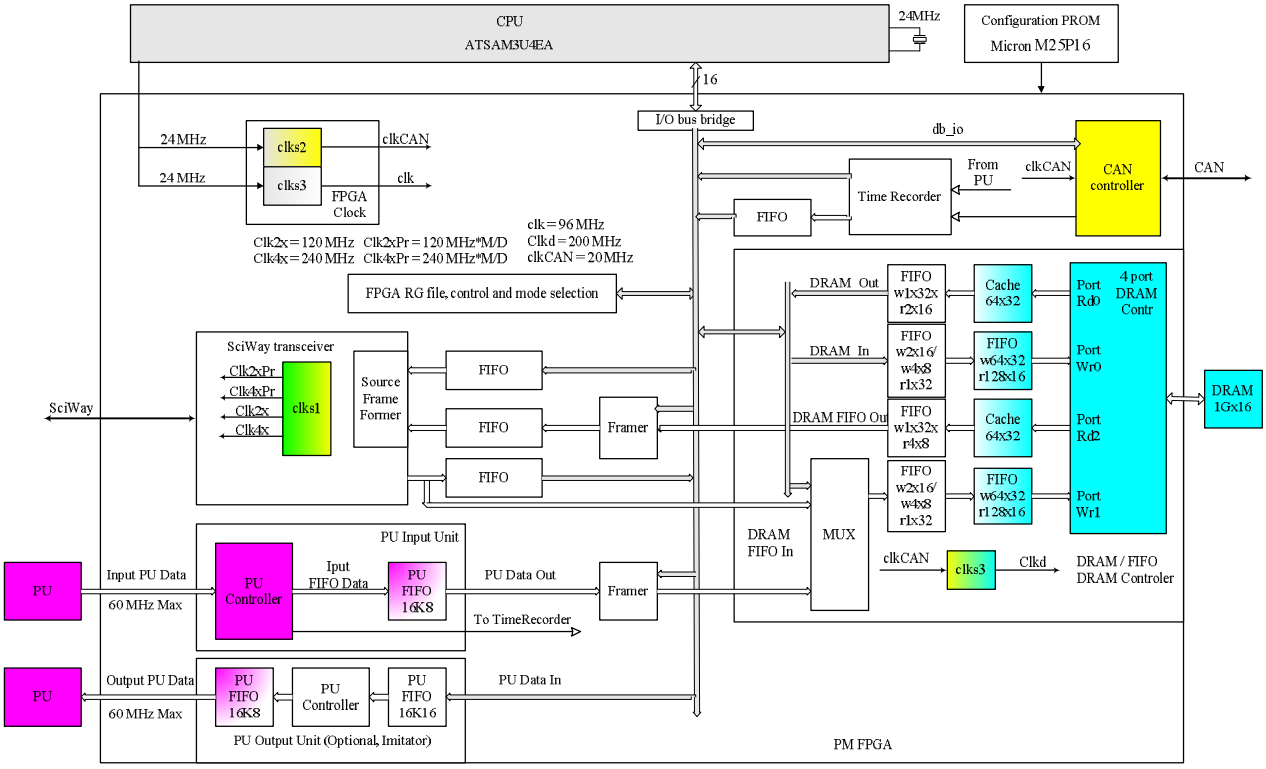

Fig. 10. Periferal Module FPGA Development Kit

V. PERIPHERAL MODULE MEMORY ARCHITECTURE

Central element of the peripheral module is a multiport dynamic random access memory of great volume. This memory can be simultaneously used as a true dynamic memory and as a FIFO memory to quick data collection from sensors on their frequencies and accumulated data issuance to SciWay transmitter (Fig. 12).

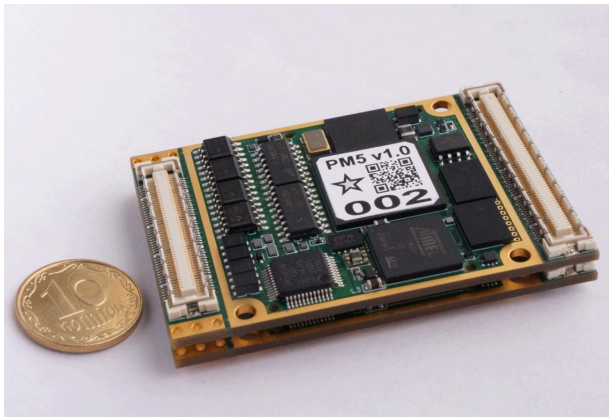

Fig. 11. Peripheral module

The memory structure allows to microcontroller program to read and to write data with addresses to memory as to RAM through separate ports and to write data through separate port with addresses to it as to FIFO. Also direct FIFO access from SciWay transmitter and receiver or scientific sensor is possible.

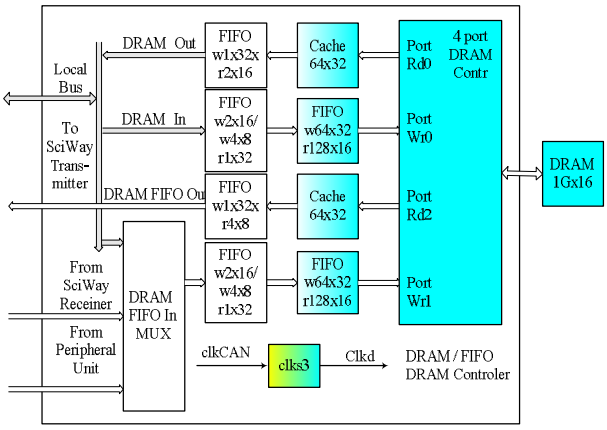

Fig. 12. Multiport DRAM

Peripheral module unification and its adaptation for work with a different type sensors that operate at different frequencies with different interfaces,, may issue the data by bites, bytes, words and packages are provided ensured by extensive use of FIFO and FIFO chains that are located on FPGA module FPGA between its units. Often these FIFOs are asymmetrical when written data width does not match read data widthone. Such approach allows to changechanging data formats coming from various sensors and at various frequencies. For example, a chain of two series-connected asymmetric FIFOs is used as a part of multiport dynamic random access memory:

FIFO w2x16 / w4x8 r1x32 with ability to write 16- or 8-bitwise words and to read 32-bitwise words. It is necessary to harmonize sensor and system bus width with dynamic memory controller bus one;

FIFO w64x32 r128x16 r1x32 with ability to write 32-bitwise words and to read 16-bitwise words. It is necessary to harmonize dynamic memory controller bus width with dynamic memory bus one.

To achieve maximum dynamic memory performance, reference to it is performed by blocks of data. Block size is automatically selected depending on the amount of data in a FIFO (while writing) or dynamic RAM (while reading). With increaseing of in data in FIFO or in dynamic memory, blocks volume increases too.

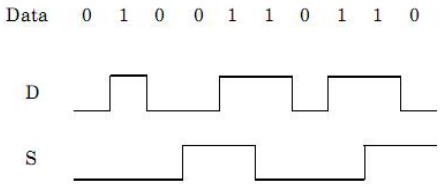

Fig. 13. Data-Strobe Code method

VI. INTERCONNECTION BETWEEN LAYERS

Interconnection between peripheral modules and central unit is performed by so called SciWay unified interface [8]. To reduce differences in data and clock income time, the so called Data-Strobe (DS) coding method is used in the interface [16], Fig. 13 illustrates its features.

Data D thus are transferred unchanged and signal S changes its value if the next bit of data repeats previous one.

The signals of peripheral modules and the central unit are asynchronous to each other. Phasing technology is used for data synchronization as illustrated by Fig. 16.

The data and clocks of transmitter are fixed by clock bundle of receiver, each clock in bundle is shifted in phase at 90 degrees with respect to the previous one. The results of this fixation are themselves fixed several times again but mostly by clocks with phase 0. As a result 4 bit binary line code is formed which allows us to exactly determine the receipt time of transmitter data and clocks on the timeline of receiver exactly. Modern FPGAs allow to useusing more then than 4 phases during phasing that enables SciWay interface reliability increase.

VII. SOURCES PACKING

SciWay transceiver is designed to provide protocol microprocessor with communication with peripheral devices (sensors and actuators). Communication is carried out in the Data-Strobe (DS) mode [16]. Peripherals of one controller can be combined in network up to 32 devices. The controller works either in mode without packaging or in packaging mode with data packets according to packet telemetry standard CCSDS 102.0-B-5 [7], packet format is shown in Fig. 17.

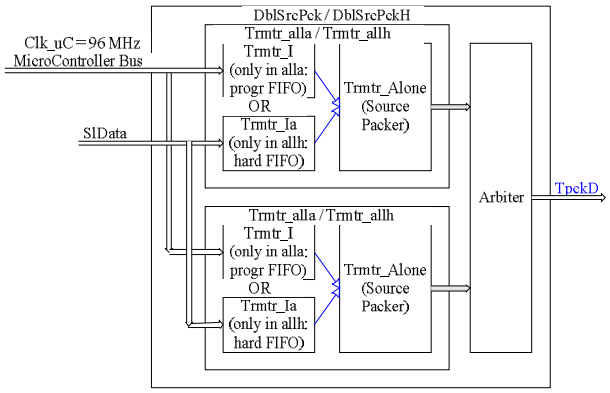

Fig. 14. Doubled source packer

VIII. TRANSPORT FRAMES

Formation of transport packages is necessary only in central block. To test system interconnection algorithms, the Framer (Fig. 15) was put to the basic version of the peripheral module. Formation of transport packages is performed according to [6]. The format of the transport frame is shown in Fig. 18.

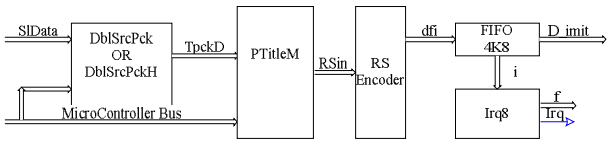

Fig. 15. Framer

Input data can be entered in the transport packet generator either from the microcontroller bus (software input) or from FPGA hardware SlData input. Mode selection is made during FPGA design and can notcannot be changed during its operation. Additional software changes of generator modes is are possible through MicroControler Bus. Microcontroller can read framer status through MicroControler Bus too.

The generator structure consists of:

output FIFO 4K8;

interrupts unit Irq8 (analyzes state of output FIFO 4K8, forms Interrupt requests at occurrence of its empty, programmable empty, full and programmable full signals);

doubled source package generator DblSrcPck or DblSrcPckH for software or hardware input respectively;

transport package title generator PTitleM;

Reed-Solomon encoder RS Encoder.

Doubled sources package generator (Fig. 16) is designed to convert continuous input data stream into packages of sources information designed according to the recommendations [6].

Doubled source package generator includes:

two data storages for hardware (unit Trmtr_allh) or software (unit Trmtr_alla) mode of data entry;

Arbiter.

Each storage includes an input FIFO, connected either to the microcontroller bus (node Trmtr_I) or to the SlData bus (node Trmtr_Ia) and actual source packages generator Trmtr_Alone.

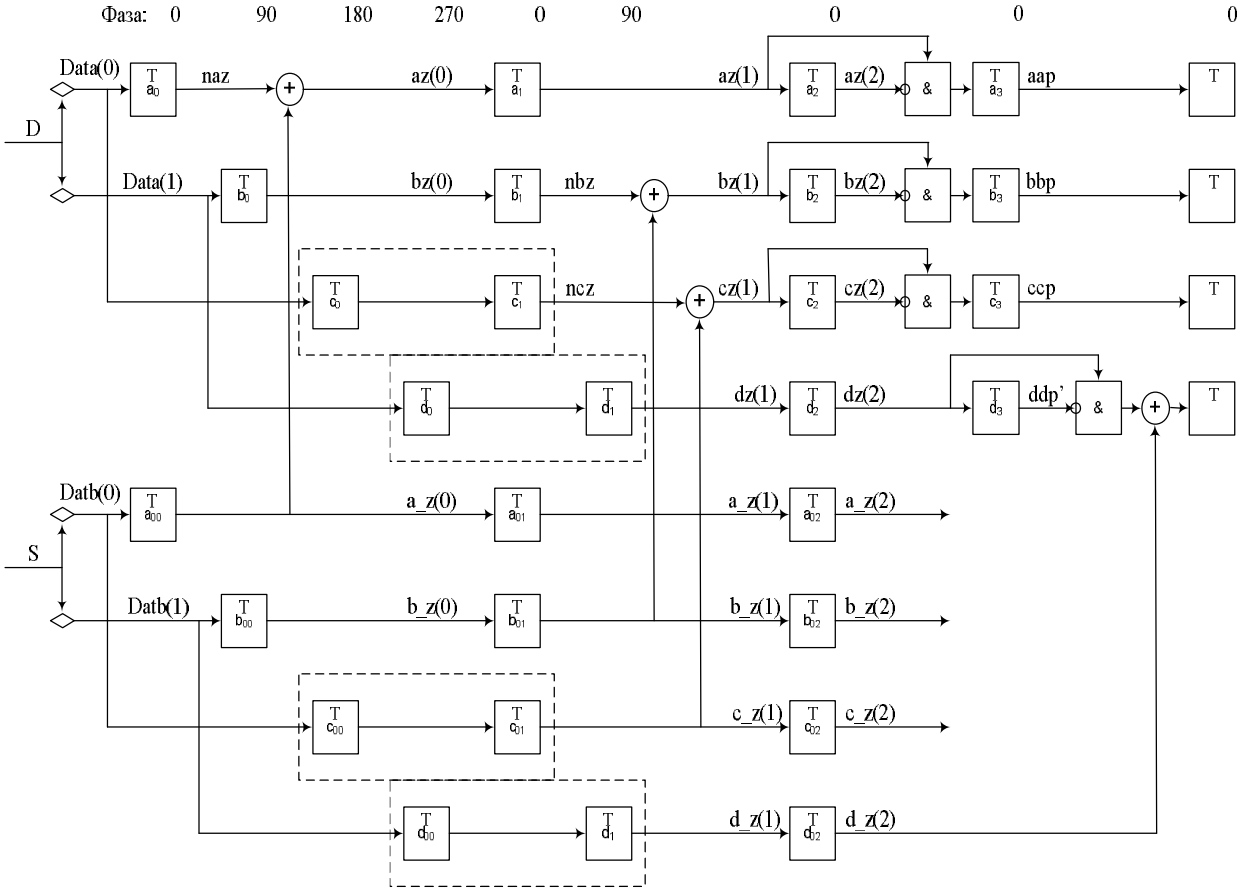

Fig. 16. Data phasing method

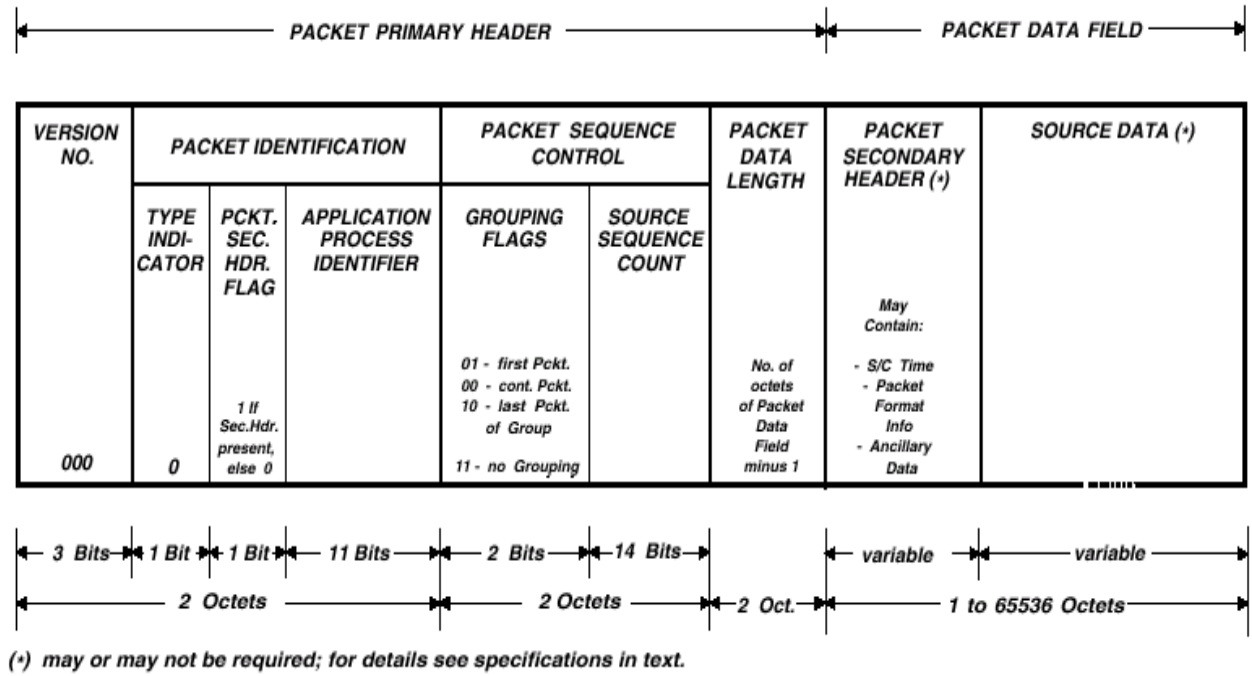

Fig. 17. Source pack

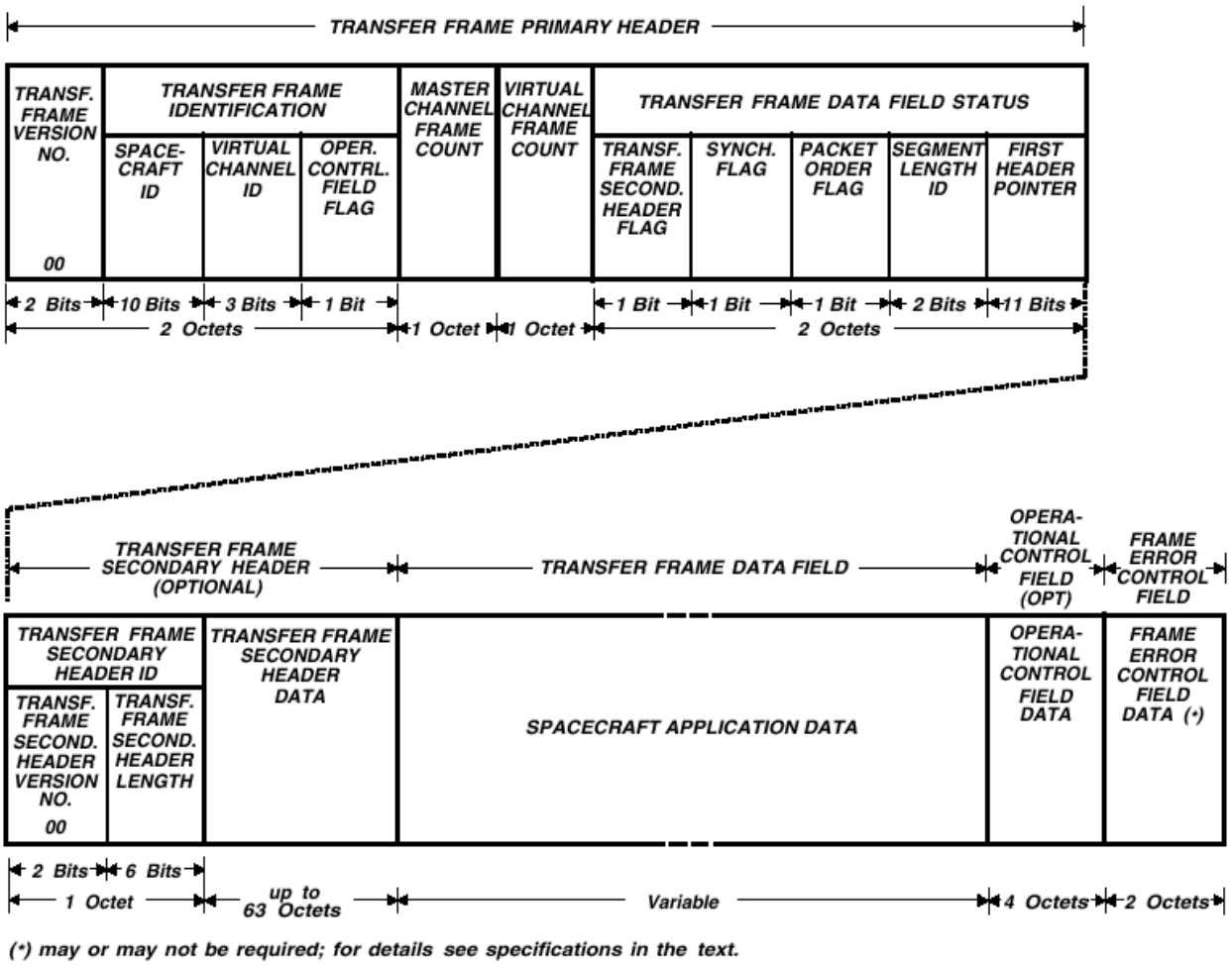

Fig. 18. Transport frame

Storage and generator together work similar to SciWay synchronous channel transmitter (see. Section 7).

When packages are ready at the generators output, the arbiter prefers one of them and broadcasts its package on outgoing bus TPckD.

PTitleM unit is intended to form headers for transport packets [6].

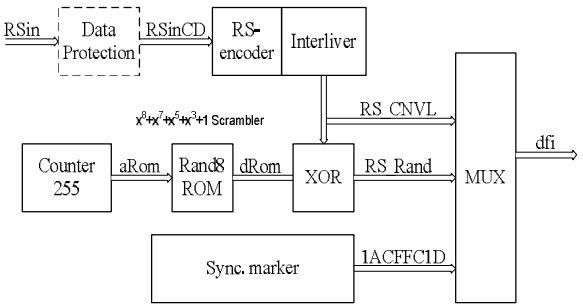

Fig. 19. Reed-Solomon encoder

Reed-Solomon encoder (Fig. 19) is intended for error detection and correction providing when errors occur during transport packages transmission and for transport frames formation from incoming sources packets. Detection and correction of errors is performed according to [6].

The structure of the Reed-Solomon encoder includes:

own Reed-Solomon encoder RS-encoder;

Interliver;

modulo 255 Counter;

scrambling Rand8 ROM;

XOR unit;

Synchronization Marker generator;

output multiplexer MUX.

Own Reed-Solomon encoder RS-encoder performs transport packages noise immunity encoding according to recommendations [6].

Fig. 19 also shows a possible position of future developed data protection unit.

Appointment of other components of the Reed-Solomon encoder are is evident from their names.

IX. SYNCHRONIZATION AND TIMING

Data from a large number of sensors are processed in cyber-physical systems. This requires the solution of their synchronization and timing task. Peripheral

modules and central unit of scientific data collection and accumulation system have Time Recorder unit (Fig. 20), which provides a solution to this task. Primary this unit been used only for CAN channel transfers timing, then it turned reasonable to perform data exchange timing for each sensor and actuator.

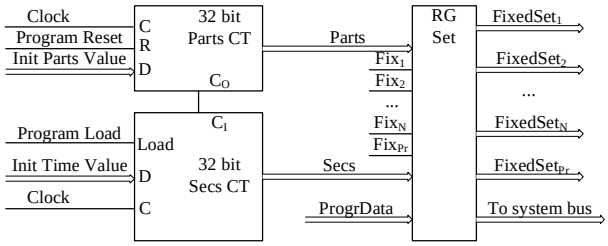

Fig. 20. Time Recorder Unit

The unit contains 32-bitwise second fractions counter Parts CT, 32-bitwise seconds counter Secs CT and memory unit (set of registers – RG Set) for fixing seconds, fractions of a second and software data. Fixation is either by sensor controller signal (Fix_1, ... Fix_N) or it can be caused by microcontroller (Fix_{Pr}). Recorded values ($FixedSet_1$, ..., $FixedSet_N$) come back to the sensor controllers and are available for microcontroller (through system bus). The microcontroller can set and correct unified system time by loading counters original values.

X. SCIENTIFIC DATA COLLECTION AND ACCUMULATION SYSTEM TESTBENCH STRUCTURE

The testbench structure [13], [17] is basic and is refined for each scientific equipment complex (SEC). The testbench structure is shown in Fig. 21.

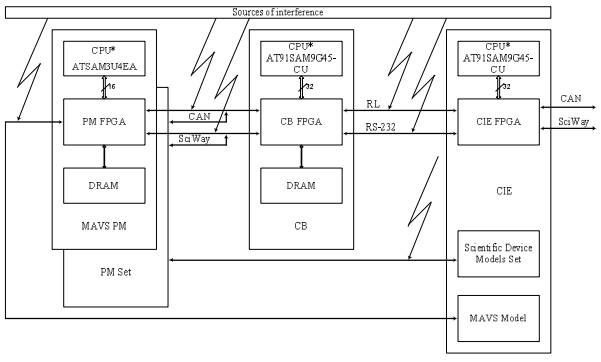

Fig. 21. System testbench

Data exchange between peripheral modules, central unit and Control and Inspection equipment through existing interfaces under external noise influence simulation is performed during scientific data collection and accumulation system design.

Microcontrollers models (*) are incomplete, they describe interface part only that allows to simulate exchanges by system buses. During simulation it is possible to change system configuration, units and interfaces parameters and quantities. Approximately, 1 microsecond of system real time is simulated in 1 second. After FPGAs topology design it is possible to determine FPGAs thermal parameters.

XI. CONCLUSION

Experience of satellite scientific data collection and accumulation system designing and debugging can be used for design of advanced cyber-physical systems.

The essential elements of these systems are:

sensor data which are to be transmitted to the cyber-physical systems next level packing;

multiportal mass memory which can be used as true memory as well as hardware and software available FIFO memory that provide sensors data collection. The work of the memory should be supported by cache memory;

FIFO chains should be used between units of cyber-physical systems to accommodate interfaces of different sensors;

sensors and actuators timing is necessary to provide;

system debugging must be maintained by test benches simulation and veryficationverification;

it is highly desirable to provide modeling with taking into account sensors and actuators interfaces parameters variations.

Scientific data collection and accumulation system developed in the Lviv Center of Institute for Space Research of NAS and SSA of Ukraine with the participation of the Computers Department of Lviv Polytechnic National University can be taken as the basis for the design of advanced cyber-physical systems.

REFERENCES

[1] Information technology – Open Systems Interconnection – Basic Reference Model: The Basic Model – Part 1. ISO/IEC 7498-1:1994(en).

[2] Hlukhov V. S. Multi-leyer computer system hardware costs evaluation (in Ukrainian). Proceedings of the National University “Lviv Polytechnic” “Computer Science and Information Technology” No. 629. Lviv, 2008. C. 13-20.

[3] Anatoliy O. Melnyk. Cyber-physical systems multilayer platform and research framework. Advances in Cyber-Physical Systems, ACPS Vol. 1, No. 1, pp. 2–7, 2016.

[4] Big data (2016, December). [Online]. Available: https://en.wikipedia.org/wiki/Big_data

[5] Microelectromechanical systems (2016, November). [Online]. Available: https://en.wikipedia.org/wiki/Microelectromechanical_systems

[6] Recommendation for space. Data system standards. TELEMETRY CHANNEL CODING. CCSDS 101.0-B-5. Blue book. June 2001.

[7] Recommendation for space. Data system standards. Packet telemetry. CCSDS 102.0-B-5. Blue book. November 2000.

[8] Hlukhov V.. Lukeniuk A., Shenderuk S. A look at satellite scientific data collection system as at cyber-physical system (in Ukrainian). The first scientific seminar “Cyber-physical systems: Achievements and Challenges”. 25–26 June 2015. Lviv, Ukraine.

[9] Hlukhov V. S., Lukenyuk A. A. and Shenderuk S. G. Unified interface of onboard spacecraft systems (in Ukrainian). Space Project IONOSAT-MICRO (in Russian) Research publication. The National Academy of Sciences of Ukraine. State Space

Agency of Ukraine. Institute for Space Research. Kyiv, "Academperiodica". 2013. Pp. 126 – 133.
[10] Hlukhov V., Lukeniuk A., Shenderuk S. The use of reconfigurable elements in on-board collecting and processing data systems (in Ukrainian) // 2nd Ukrainian Conference on Space Research. Reports. P.67. Katsiveli, Crimea, Ukraine, 2002.
[11] Hlukhov V., Lukeniuk A., Shenderuk S. // VLSI for satellite "Sich-2" scientific data collection system (in Ukrainian). Proceedings of 5-th International Conference "Advanced Computer Systems and Networks: Design and Application" ACSN-2011 / September 29 – October 01, 2011, Lviv, Ukraine. P. 57–60.
[12] Hlukhov V. S., Lukenyuk A. A. and Shenderuk S. G. Scientific data collecting system FPGA Set (in Ukrainian). Space Project IONOSAT-MICRO (in Russian) Research publication. The National Academy of Sciences of Ukraine. State Space Agency of Ukraine. Institute for Space Research. Kyiv, "Academperiodica". 2013. P. 134–139.
[13] Hlukhov V., Lukeniuk A., Shenderuk S. // On-board collecting scientific information system FPGA Set (in Ukrainian). Proceedings of IX International Conference "Gyrotechnology, navigation, movement control and aerospace technic engineering". Reports. 17–18 April, 2013. Kyiv, Ukraine. p. 401–409.
[14] Hlukhov V., Lukeniuk A., Shenderuk S. Dedicated controller for satellite "Sich-2" scientific information collection (in Ukrainian) // Proceedings of the Lviv Polytechnic National University "Computer Systems and Networks". – Lviv, 2011. – No. 717. – P. 10–16.
[15] Data Flow in the OSI Model. (2016, December). [Online]. Available: https://technet.microsoft.com/en-us/library/cc977591.aspx
[16] Space engineering. SpaceWire – Links, nodes, routers and networks. ECSS Secretariat ESA-ESTEC Requirements & Standards Division. Noordwijk, The Netherlands. 24 January 2003. ECSS--E--50--12A. ESA Publications Division. ESTEC. Copyright 2003 E by the European Space Agency for the members of ECSS.
[17] V. Hlukhov. A. Lukeniuk, S. Shenderuk. Simulation of FPGA system for gathering scientific information (in Ukrainian) // Proceedings of 14-th International Scientific and Practical Conference "Modern information and electronic technologies" MIET-2013, Odessa, 27–31 May, 2013. P. 131–134.

Valerii S. Hlukhov is a professor of the Department of Computer Engineering in Lviv Polytechnic National University, Ukraine. He graduated from Lviv Polytechnic Institute with the engineer degree in computer engineering in 1977. In 1991, he obtained his Ph.D. from the Institute of Modeling Problems in Power Engineering of the National Academy of Science of Ukraine. He was recognized for his outstanding contributions to special-purpose computer systems design as a Fellow Scientific Researcher in 1995. He was awarded the academic degrees of doctor of technical sciences in 2013 in Lviv Polytechnic National University. He became a Professor of Computer Engineering in 2014. He has scientific, academic and hands-on experience in the field of computer systems research and design, proven contribution into IP Cores design methodology and high-performance reconfigurable computer systems design methodology. He is experienced in computer data protection, including cryptographic algorithms, cryptographic processors design and implementation. Mr. Hlukhov is an author of more than 100 scientific papers, patents and monographs.

Adolf Lukeniuk, Ph.D., specialty major Technical Ccybernetics (1981), Director of Lviv Centre of Institute for Space Research of National Academy of Sciences and the State Space Agency of Ukraine. In 1969, he graduated from the Lviv Order of Lenin Polytechnic Institute on specialty anmajoring in electrical engineering. From 1969 to 1997, he was junior researcher, senior engineer, chief designer, head of special engineering and design bureau of Physico-Mechanical Institute of the NAS of Ukraine. From 1997 to present he works in the Lviv cCenter of Institute for Space Research of NAS and the SSA of Ukraine as Deputy Director for Scientific Affairs and as Director. He is author of more than 60 scientific papers and 40 patents.

Sergii G. Shenderuk is Department Chief Head in Lviv Centre of Institute for Space Research of National Academy of Sciences and the State Space Agency of Ukraine. In 1986, he graduated from the Lviv Order of Lenin Polytechnic Institute on specialty ofmajoring in Radio Engineering. From 1986 to 1997, he was Engineer, Design Engineer in special engineering and design bureau of Physico-Mechanical Institute of the NAS of Ukraine. From 1997 to till present, he has been works working in the Lviv Ccenter of Institute for Space Research of NAS and SSA of Ukraine in positions ofas chief engineer, junior researcher, researcher, head of department. He is the author of more than 10 scientific papers.

ACKNOWLEDGEMENT

The scientific results, presented in this article, were obtained within the frame of research project "The integration of methods and tools for measurement, automation, processing and protection of information in the base of cyber-physical systems" number 0115U000446, 01.01.2015–31.12.2017, financially supported by the Ministry of Education and Science of Ukraine.