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SIMULATION AND INVESTIGATIONS OF A SOFTWARE IMPLEMENTED PHASE-LOCKED LOOP WITH IMPROVED NOISE IMMUNITY

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Abstract: The improvement of noise immunity of a communication system is an effective way to increase the capacity of communication systems, which would provide more qualitative service for a larger number of users. This task can be solved by lowering the noise threshold of a phase-locked loop (PLL) in these systems if the dynamic properties of the device are preserved. The literature review indicates that such a device with improved noise immunity has already been implemented, but the effects of noise and modulation on its dynamic behavior were analyzed separately. This article is devoted to the analysis of the behavior of a digital firmware PLL under the simultaneous influence of noise and modulation of the input signal. The article depicts the structure of the classical digital PLL and its modifications and explains key differences between them.

The simulation of the classical PLL with either absence or presence of noise at the device input was carried out. The simulation results show that the PLL is not able to detect all phase changes when the noise is present. Besides, the modified PLL has a wider working frequency range than the classical one under noisy conditions. The investigations of the PLL dynamic behavior with the simultaneous influence of random noise and Binary Phase Shift Keying (BPSK) modulated input signal was performed. The results of the research show that the duration of the transient processes during the processing of the BPSK modulated signal in the modified device is at least twice as low as that for the classical one. In addition, the number of errors during the signal detection increases faster for the classical PLL than for the modified one when the noise level rises. The use of the modified PLL in modern communication systems gives an opportunity to increase their capacity.

Key words: firmware phase-locked loop (PLL), modified phase detector, binary phase-shift keying (BPSK) modulation, additive white Gaussian noise (AWGN)

1. Introduction

Nowadays, phase-locked loops (PLL) are versatile devices used in radio-electronic systems of different purposes for solving a wide range of tasks from frequency synthesis and pulse generating to detecting signals with binary phase-shift modulation [1–3].

The use of new quadrature modulation methods gives a possibility of using frequency band in communication systems more efficiently, increasing the number of its users and making the operation of the system cheaper.

The further development of communication systems is restrained by the threshold value of the signal-to-noise ratio (SNR), exeeding which makes the system ineffective. The threshold value of the SNR affects the capacity of the communication system which is determined by the modified Vitterbi formula [4].

Numerous theoretical studies of phase-locked loops show that there is a contradiction between the choice of device parameters to ensure its high noise immunity and the ability to monitor modulated signals [5, 6]. The increase in the device bandwidth gives an opportunity to receive signals with a large modulation index, but makes it vulnerable to external noise and vice versa.

This contradiction was solved in papers [7–9]. These works present criteria of choosing optimal PLL parameters to reach the maximum threshold noise intensity and the maximum hold-in range. These works also offer the method of the improvement of PLL noise immunity, which consists in using a modified phase detector with additional narrow-band filtering of a useful signal from noise.

The simulation studies carried out in this paper have shown that the noise threshold of the modified PLL is significantly reduced for signals with high modulation index, while nonlinear signal distortions at the output of the device are reduced. The indicated results proved their practical value in works [10, 11] which show the efficiency of using a PLL with a modified phase detector in systems with quadrature modulation and GPS systems.

In the above mentioned works, the object of the study was the analog PLL, and the research methods were limited to the simulation. The described above studies were improved in work [12], which presents a firmware implemented PLL with high noise immunity and experimental investigations of its boundary noise immunity. The results of the study show that the digital PLL (created according to the analog prototype) with a modified phase detector has a lower noise threshold of up to 2.5 dB and has better dynamic properties comparing to the classical PLL. However, during the

research, the influence of external noise and phase manipulation on the synchronization of the device was analyzed separately.

Therefore, the purpose of this article is to analyze the noise immunity of the firmware implemented PLL under the conditions of simultaneous influence of external noise and modulated signal at the input of the device.

2. Structure of the classical and modified digital PLL

This work investigates two types of a digital PLL. The classical PLL is the first of them and its block diagram is shown in Fig. 1. It consists of a phase detector (PD), a digital filter (DF) and a voltage-controlled oscillator (VCO), all of them being software implemented.

This PLL contains a first order digital recursive filter which is the prototype of an analog passive lead-lag filter. The coefficients of the filter are determined by the cutoff frequency f_c and the coefficient of proportionality m, calculated by the formulas given in [13].

Other parameters of the PLL are K_{PD} and K_0 being the coefficients of transmission of PD and VCO respectively. These parameters determine the hold-in range of the device [14, 15] and affect the form of the PLL frequency response [13].

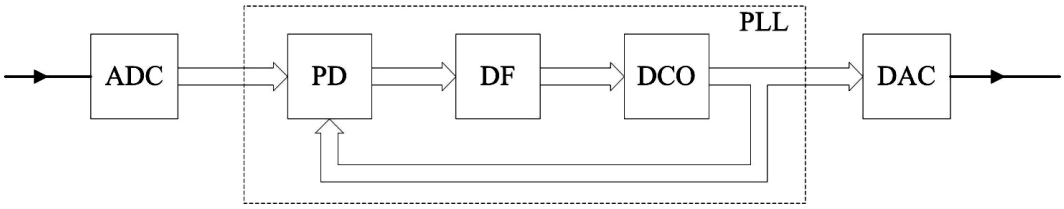


Fig. 1. Block diagram of the classical digital PLL [12].

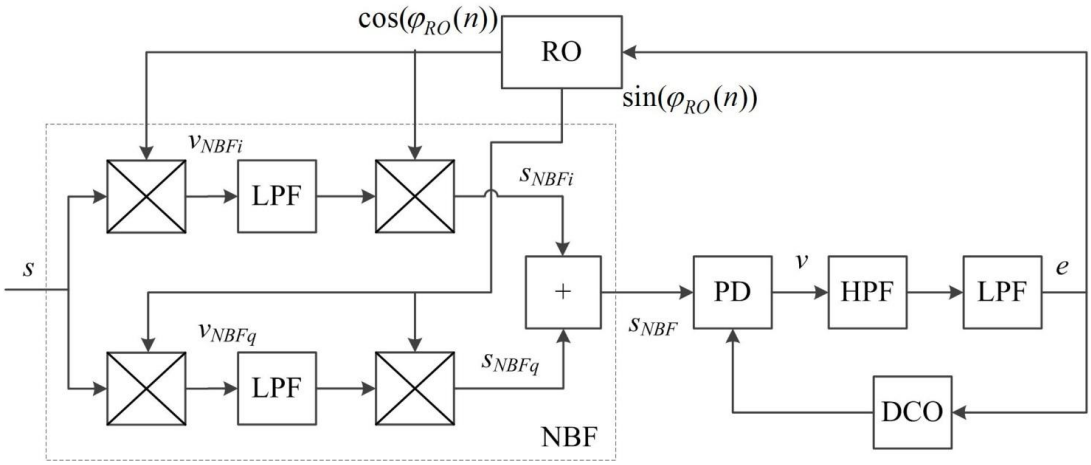


Fig. 2. The block diagram of the digital PLL with the modified phase detector [12].

The second type of a device considered in this article is the modification of the first one (Fig. 2). It contains an additional narrowband filter unit (NBF), whose purpose is to maximize the filtering of noise at the device input. An additional high-pass filter (HPF) is included between the phase detector and the loop filter to compensate for the suppression of changing the dynamics of a useful signal.

To restore the spectrum of a useful signal correctly without distortion, the amplitude frequency response characteristics of the NBF and HPF should be matched with each other (Fig. 3). This is possible if the coefficients of proportionality of the two filters are the same and their cutoff frequencies are determined by the ratio $f_{HPF} = f_{NBF} / m_0$. The mathematical model of such a device is described in detail in [12].

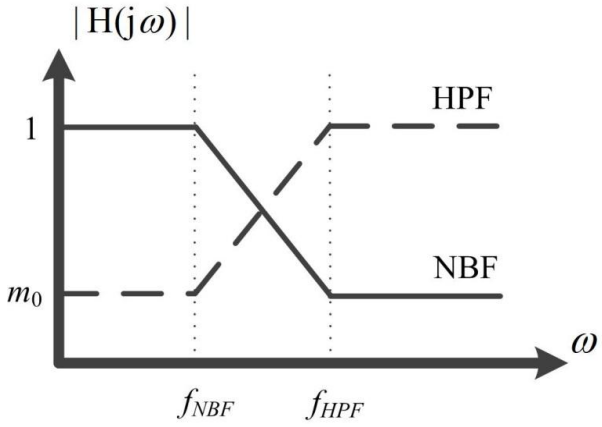


Fig. 3. Frequency response of the narrow-band filter and the high-pass filter [12].

3. Simulation of the digital PLL

One of the aspects of this work is the simulation of a radio communication system using the PLL with a modified phase detector. The investigation of this system by its simulation is a necessary task before its firmware implementation. A Matlab Simulink software package was chosen as a modelling system.

The investigated simulation model contains the following elements (Fig. 4):

- source of modulated signal;
- communication channel with additive noise;
- signal detector implemented on the basis of a PLL with the detuning of variable frequency γ.

The simulation was carried out using signals with BPSK modulation. BPSK is the simplest type of digital phase modulation. When this type of modulation is used, the signal amplitude changes from "0" to "1" with the signal phase changing. The random digital signal generated and modulated according to this rule was used in further simulation.

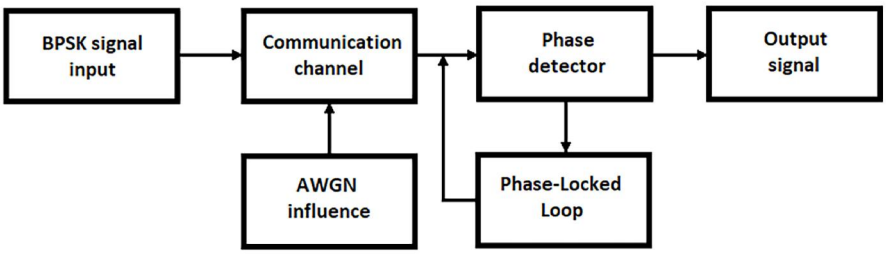
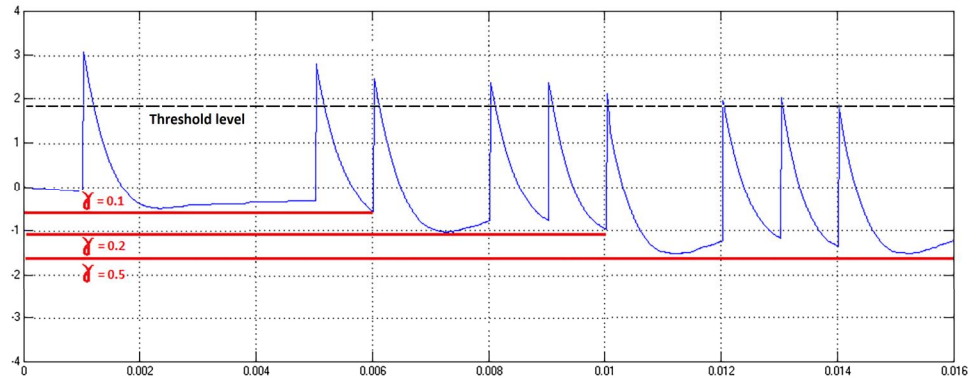
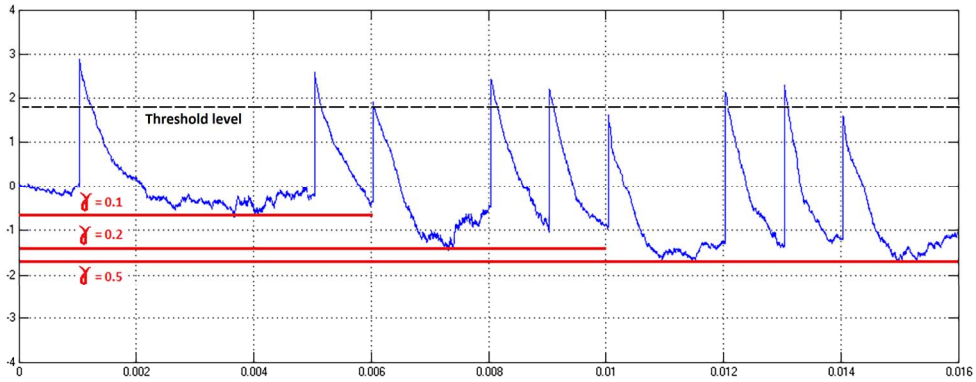


Fig. 4. Block diagram of the simulation model.



a



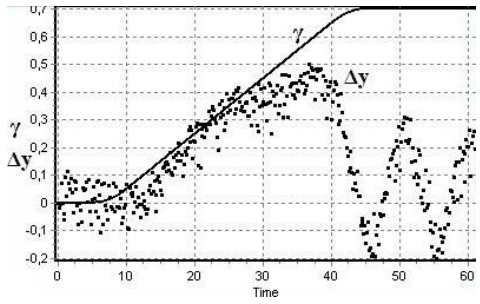
b

Fig. 5. BPSK signal detected for various values of frequency detuning under the conditions of absence (a) and presence (b) of additive noise in a communication channel.

The research was carried out in the cases of absence and presence of noise in a communication channel. The aim of the research is to determine the behavior of the detected signal depending on the change in frequency detuning γ. The range of the values of frequency detuning γ is from 0.1 to 0.5. The results of the simulation are presented in Fig. 5. The first plot (Fig. 5a) shows the results of the detection of the BPSK signal in the case of the absence of noise in the communication channel. The second plot (Fig. 5b) depicts the results of BPSK signal detecting under the condition of the additive white Gaussian noise (AWGN) in the communication channel. The signal-to-noise ratio equals 7 dB. At the threshold level of the detection 1.8 we can recognize all phase changes, even with different values of frequency detuning. But after the influence of the additive noise in the communication channel, two phase changes are unrecognizable (at 0.01 s and at 0.014 s).

The results of simulation also indicate that the amplitude of the detected signal increases with the increase in frequency detuning γ and noise power in the communication channel. The similarity of the signal behavior during the change of frequency detuning in the experimental device with the simulation results confirms the adequacy of this implementation.

In addition to the described simulation of synchronization process with equal fixed levels of normalized frequency detuning γ, a simulation of the gradual change of this detuning from 0 to 0.7 from the hold-in range value was also carried out [16] (Fig. 6). In radar systems, such a change corresponds to the uniformly accelerated target motion, and in the communication system it corresponds to the movement of the user.



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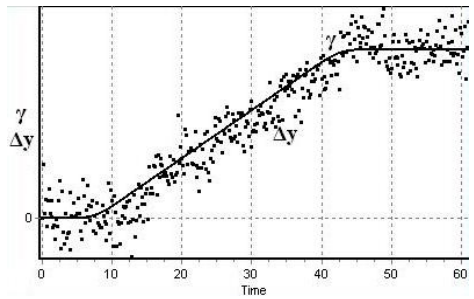


b

Fig. 6. The simulation of the hold-in range in classical (a) and modified (b) PLL.

The results of simulation taking into account the combined effect of regular frequency detuning and additive noise showed that in the classical PLL the loss of synchronization occurred at the level 0.4 of the hold-in range value (Fig. 6a), and the modified device, regardless of somewhat worse phase error variance, keeps synchronization in the entire given frequency range (Fig. 6b).

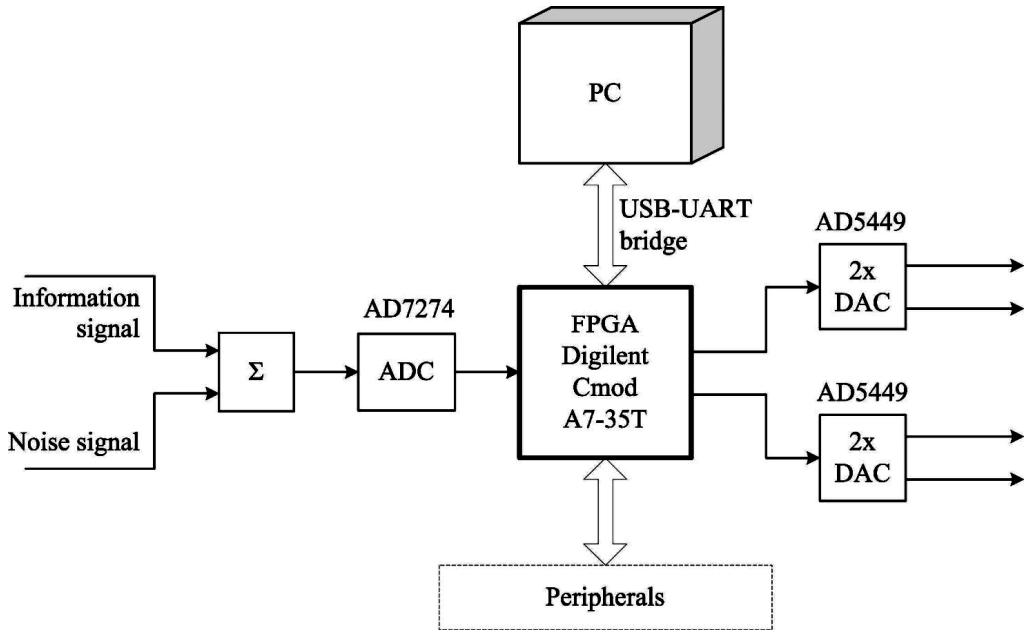


Fig. 7. Block diagram of firmware implementation of the PLL [12].

4. Firmware implementation of the digital PLL

Both classical and modified devices were implemented on a Cmod A7-35T development board with the Field-Programmable Gate Array (FPGA) Xilinx Artix-7 [17]. FPGAs exceed most standard microcontrollers in operation speed, and their parallel structure enables them to perform multiple operations simultaneously (which microcontrollers can only perform sequentially). All those features facilitate their research.

The board itself does not include built-in analog-to-digital (ADC) and digital-to-analog converters (DAC). Therefore, the implemented devices include 12-bit ADCs (AD7274) and DACs (AD5449), as well as smoothing filters and an adder, which is built on the basis of the operational amplifier AD8615 (Fig. 8).

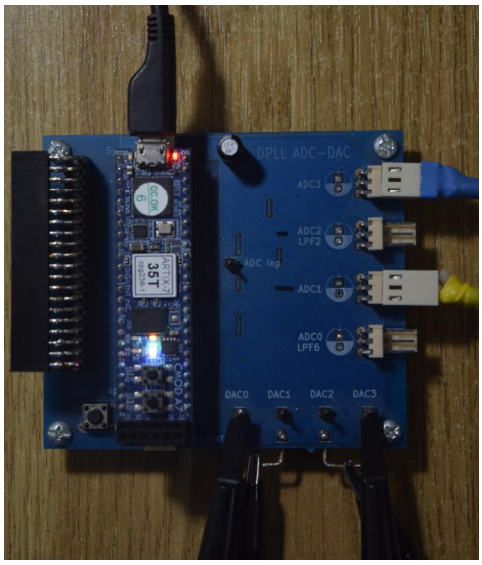


Fig. 8. Setup for experimental research of firmware implemented digital PLL.

Fig. 8 shows the photograph of the board of implemented device. Inputs of the device are located on the right side of the board and its outputs are on the bottom of the board. The FPGA is connected to a PC via a USB cable (on the top). Pinouts on the left of the board are designed to connect them to logic analyzer for adjusting the device.

The software part of the device was developed in the Xilinx Vivado environment, and the interface between the PC and the FPGA is modelled in MATLAB environment. In MATLAB environment makes it possible to change the parameters of each component of the device and the type of the phase detector (classical or modified), as well as to determine the set of output signals to be observed on the oscilloscope.

5. Experimental study of the PLL dynamic behavior under the influence of modulation and noise

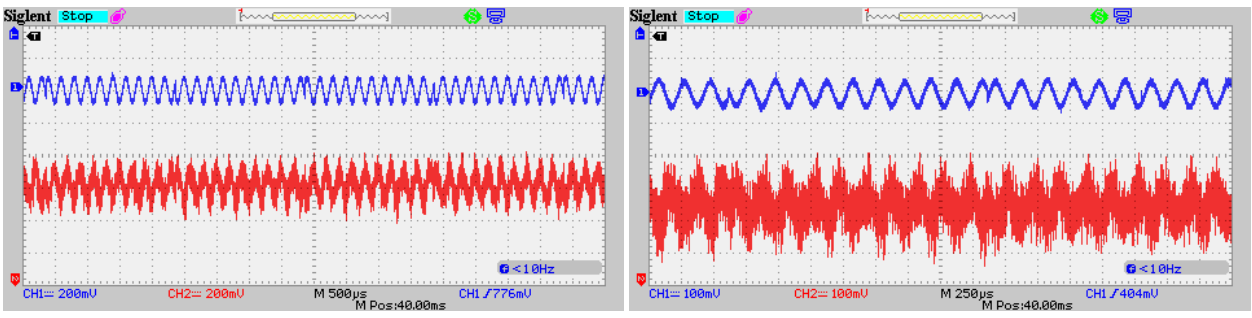
The influence of the modified PD on the PLL dynamic behavior has already been investigated in [12]. However, the above-mentioned study was conducted under the noise-free conditions. In this experiment, input signal is the mixture of the BPSK modulated signal and additive Gaussian noise. As well as in the previous work, the goal of the experiment is to compare the duration of the transient processes at the output of the digital loop filter occurring during a phase step of the input signal for classical and modified PLLs. Another task was to estimate the magnitude of this signal in steady state for both cases to compare the efficiency of noise suppression in the device.

Experimental studies were carried out for the following values of device parameters:

- Loop gain $K = K_0 K_{PD} = 5000$ s^{-1};
- DF cutoff frequency $f_c = 50$ Hz;
- DF coefficient of proportionality $m = 0.005$;
- NBF coefficient of proportionality $m_0 = 0.1$;
- NBF cutoff frequency $f_{NBF} = 20$ Hz;
- HPF cutoff frequency $f_{HPF} = 200$ Hz;
- Sampling rate $F_s = 100$ kHz.

Parameters of the input useful signal are:

- carrier frequency $f = 5$ kHz;
- modulation frequency of the BPSK modulated signal is 10 Hz;
- normalized amplitude of the signal is 1.25 V.



a *b*

Fig. 9. PLL input signal with SNR: a – 5 dB; b – 1 dB.

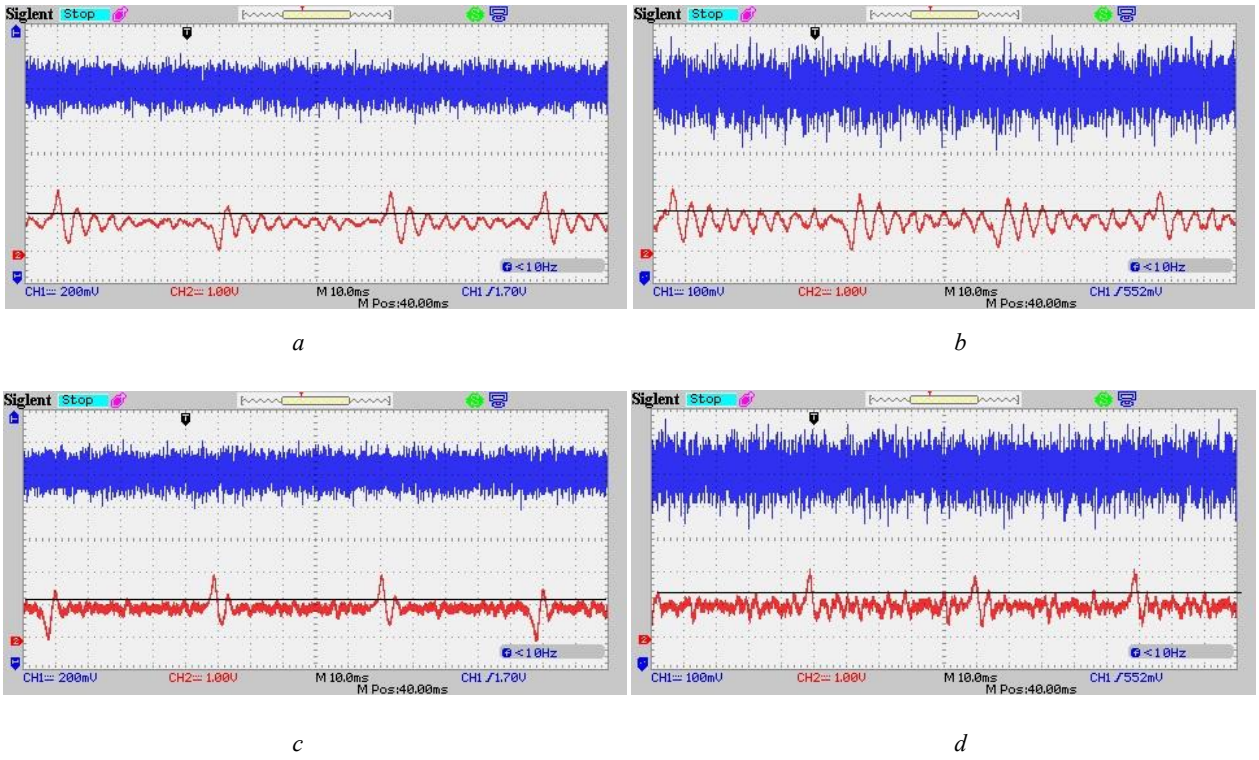


Fig. 10. Output signal of the digital loop filter and a threshold level of detection for classical (a,b) and modified (c,d) PLL with input SNR: 5 dB (a,c); -1 dB (b,d).

The signal fed to the device input is shown in Fig. 9. The left image (Fig 9a) corresponds to SNR equalling 5 dB and the right one (Fig 9b) to SNR equalling -1 dB. The noise-free signal is shown at the top of the figure, and mixture of useful signal and additive Gaussian noise is shown below.

SNR adjustment is achieved by changing the amplitude of the input signal. Since the amplitude of the signal affects PLL hold range, the input mixture of the useful signal and the noise is normalized by software, so that the amplitude of the useful signal might be equal to 1.25 V.

The results of observations are represented in Fig. 10. Fig. 10a and 10b illustrate the shapes of output signal from LPF for classical PLL and Fig. 10c and 10d for the modified PLL. PLL makes a decision about the reception of digitalised information based on a threshold principle. In the case of higher SNR values (Fig. 10a and 10c), the number of errors of signal detection with the use of the classical and modified device is approximately the same, but the duration of the transient process caused by the phase steps of the input signal in the modified device is at least two times smaller than in the classical device. In the case of lower SNR values (Fig. 10b and 10d) it is difficult to compare the duration of the transient processes unambiguously due to the distortion of the output signal by the noise for both devices. However, for a classical device, the number of the crossings of threshold detection level increases significantly with the increase in noise level, while the number of crossings of this level for the modified device increases more slowly.

6. Conclusion

This work analyzes the simultaneous influence of the modulation of the input signal and noise on the behavior of the digital firmware implemented PLL. The research was conducted by means of simulation, as well as on the experimental device. The results of studies show that under the same noisy conditions the modified device can keep its synchronization in a wider frequency range than the classical one. During processing the BPSK modulated signals transient processes in the PLL with a modified phase detector are at least twice faster than in the classical PLL. In the case of low signal-to-noise ratio, the modified device makes fewer mistakes during signal detection, because the number of crossings of the threshold level is smaller than for the classical device. Thus, the modified device having a higher potential noise immunity [12] also provides better signal detection and dynamic properties in the case of the simultaneous influence of the modulated signal and noise fed to its input.

The use of such a device in the modern communication systems gives an opportunity to increase the capacity of these systems and to provide a qualitative connection for a larger number of users.

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ІМІТАЦІЙНЕ МОДЕЛЮВАННЯ ТА ЕКСПЕРИМЕНТАЛЬНЕ ДОСЛІДЖЕННЯ ПРОГРАМНО РЕАЛІЗОВАНОГО ПРИСТРОЮ ФАЗОВОГО АВТОПІДСТРОЮВАННЯ ЧАСТОТИ З ПІДВИЩЕНОЮ ЗАВАДОСТІЙКІСТЮ

Андрій Бондарєв, Іван Максимів, Сергій Алтунін

Підвищення граничної завадостійкості системи зв'язку є одним із способів підвищити місткість системи зв'язку, що дає можливість забезпечити якісний зв'язок для більшої кількості користувачів. Цю задачу можливо вирішити шляхом пониження шумового порогу пристрою фазового автопідстроювання частоти (ФАПЧ), який використовується у цих системах, за умови збереження динамічних властивостей пристрою. В літературному огляді вказано, що такий пристрій з підвищеною завадостійкістю було реалізовано, проте вплив випадкових завад та модуляції на його роботу розглядався окремо. Ця стаття присвячена аналізу поведінки цифрового програмно-апаратного пристрою ФАПЧ за умови одночасної дії випадкових завад та модуляції вхідного сигналу. В статті зображено будову класичного цифрового пристрою ФАПЧ та його модифікації і пояснено ключові відмінності між ними. Проведено імітаційне моделювання класичного пристрою ФАПЧ для випадків відсутності та присутності випадкової завади на вході пристрою. Результати моделювання показують, що пристрій ФАПЧ не здатний відстежити усі зміни фази вхідного сигналу за умови присутності шуму. Крім того, модифікований пристрій має ширший робочий частотний діапазон у завадовій обстановці, ніж класичний. Проведено експериментальне дослідження динамічної поведінки пристрою ФАПЧ за одночасної дії випадкових завад та

двійкової фазової маніпуляції вхідного сигналу. Результати дослідження показали, що тривалість перехідних процесів при обробці BPSK сигналу в модифікованого пристрою як мінімум вдвічі менша, ніж для класичного пристрою. Крім того, кількість помилок при детектуванні вхідного сигналу зростає швидше для класичного пристрою, ніж для модифікованого, коли збільшується потужність шуму. Використання модифікованого пристрою ФАПЧ у сучасних системах зв'язку дасть змогу підвищити їхню місткість.

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