TRANSFORMING AND PROCESSING THE MEASUREMENT SIGNALS

FEATURES OF IMPLEMENTATION OF RECURRENT LOGARITHMIC ADCs

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Abstract. This work is devoted to the study of the features of the implementation of recurrent logarithmic analog-to-digital converters (LADC). The general principles of construction of recurrent LADCs are outlined. The implementation of recurrent LADC with a constant and a variable in the process of converting the base of the logarithm is considered. Generalized structural schemes of the recurrent LADCs are given, and their accuracy and speed of operation are evaluated. Changing the base of the logarithm leads to a significant increase in the speed of the recurrent LADCs, and it is advisable to change the base according to the binary law. An increase in the number of conversion cycles in the recurrent LADCs with a variable base of the logarithm made it possible to obtain an accuracy higher than the nominal value of the source code. For example, in the 8-bit recurrent LADC, the accuracy of 10 binary digits is obtained in 4 conversion cycles. Exceeding the nominal value by more than 2-4 binary digits is practically impractical due to a significant increase in conversion time.

Key words: Recurrent logarithmic ADCs, principles construction, constant base, variable base, accuracy, conversion time

1. Introduction

Currently, a huge number of ADCs have been developed, which serve as an intermediate link that connects a wide variety of computerized systems with objects of control and management. The rapid development of the ADC was due to the digital processing of information and the analog form of the output signals of the vast majority of sensors. ADCs are divided into linear and non-linear. Virtually all non-linear ADCs are logarithmic. Until recently, LADCs were inferior to linear ADCs both in terms of the number of realized classes (serial, bit-by-bit, flesh) and in terms of metrological characteristics (accuracy, speed). With the development of LADCs on switched capacitors, which were patented by us from Lviv Polytechnic National University [1], the situation changed: LADCs fully achieved all the properties of linear ADCs [2 – 10]. However, we note that ADCs have several well-known advantages over linear ADCs, in particular, a much wider dynamic range of input signals, a constant value of the relative error in the conversion range, and the possibility of processing signals in logarithmic arithmetic. The latter makes it possible to significantly increase the speed of systems by reducing long-term linear arithmetic operations (multiplication, division) to fast logarithmic operations (addition, subtraction). This is especially important for real-time systems such as control systems for technological processes and robot movement, telecommunications, aeronautical, space, and others, in which information processing time must be minimized.

2. Drawbacks

LADCs on switched capacitors are realized both with a constant and with a variable in the process of transformation with a logarithm base. According to the conversion algorithm, these LADCs are sequential, with successive approximation, flesh, pulse feedback, and recurrent. The latter is currently the least studied. In the method of analog-digital conversion using a neural network, it is proposed a recurrent algorithm to increase performance [3]. In [4], compensation of the zero offsets of the analog-to-digital converter is carried out by a neural decoder, which is based on a recurrent algorithm. In [5], a model of the primary measuring transducer based on a neural network was described, in which the accuracy was increased due to a recurrent work algorithm. In the patent [6], the accuracy and speed of LADC are increased due to a recurrent transformation algorithm.

Among modern studies of converters on switched capacitors, linear ADCs based on the Dixon pump [7 – 10] are noted, in which intermediate conversion of voltage into the current is carried out. Due to this approach, the design is simplified, and manufacturability increases while implementing devices as integrated circuits. In the ADC [7], low-level signals are amplified by a Dixon pump, and time is quantized by simple functional nodes. Topologies of charge pumping are described in the textbook [8], which provides recommendations for optimizing technical solutions for ultra-low-power devices. The implementation of a linear ADC based on the Dixon pump [9] made it possible to implement the converter without analog amplifiers and current sources. In [10], a simple technique for designing converters based on charge pumps to reduce energy consumption is outlined.

The shortcomings of the above-mentioned publications are the insufficient completeness of studies of the principles of construction, the influence of the base of the logarithm, and the number of conversion cycles on the metrological characteristics of recurrent LADCs.

3. Goal

The purpose of this work is to study the principles of building recurrent LADCs and evaluate the dependence of their accuracy and speed based on the logarithm to simplify the design and implementation of converters with given parameters.

4. Implementation of recurrent logarithmic ADCs

The implementation of recurrent LADCs significantly depends on the method of creating the required number of reference values, the values of which are determined by the base of the logarithm. In turn, the base of the logarithm in the transformation process has both a constant and a variable value.

General principles of construction of recurrent logarithmic ADCs

The essence of the recurrent logarithmic analog-digital conversion is reduced to the following. By dividing the reference voltage (U_r), some reference voltages are reproduced $U_1 \div U_n$:

$$U_1 = b^{e_n} U_r;\ U_2 = b^{e_{n-1}} U_r;$$

$$U_3 = b^{e_{n-2}} U_r; \ldots U_{n-1} = b^2 U_r \quad \text{i} \quad U_n = bU_r, \qquad (1)$$

here b is the base of the logarithm, b^{e_i} is the division coefficient on the outputs of the voltage divider 1 – n, which changes accordingly i = n, n-1, n-2,...2, 1. Transformations are carried out cyclically. In the first conversion cycle, reference voltages are alternately compared with the U_{in} input voltage, starting from the first (U_1). If the comparator worked during the comparison process, then this value of the reference voltage is discarded and in the next cycle of the conversion, the next reference voltage (U_2) is compared with the input voltage, etc. If the comparator did not work during the comparison U_1, then this level of the reference voltage U_1 is memorized and in the second cycle, it is brought U_1 to the input of the voltage divider as a new reference voltage, etc. Thus, after the end of the conversion in the first cycle, a compensating voltage U_{cv_1} will be formed at the input of the voltage divider, which will serve as a new reference voltage for the second conversion cycle. In subsequent cycles, the transformation processes proceed similarly. The conversion process ends with a cycle in which the compensation voltage becomes less than or equal to the input voltage ($U_{cv} \le U_{in}$). Finally, the compensating voltage U_{cv} becomes equal to the product of the reference voltage U_r and the division coefficients of those conversion cycles in which there was a logical "1" at the output of the comparator Km, and the output code of the recurrent LADC is equal to the sum of the exponents of the power of these division coefficients.

A simplified structural diagram illustrating the essence of recurrent logarithmic analog-digital conversion is shown in Fig. 1. With the "Start" signal, the recurrent LADC is set to its initial position, in particular, the keys SW0, SW1, SW2 are turned on. Note that when keys SW1 and SW2 are on, then SW3 and SW4 are off, and conversely. Through the switched-on key SW0, the value of the reference voltage U_r is recorded in EM1, which is fed from the output of EM1 through the switched-on key SW1 to the input of the voltage divider VD and the second input of the comparator Cmp. The voltage at the first VD output takes on a value:

$$U_{cv_1} = U_r b^{e_n} \qquad (2)$$

and through the switched-on key SW2 is recorded in EM2. After the end of the "Start" signal, the cycle-by-cycle conversion begins. Each conversion cycle has some clocks, which are equal to the number of recurrent LADC bits (n). With each clock pulse, the inputs of the Cmt switch are connected alternately to the VD outputs, starting from the first output.

The compensation voltage (U_{cv}) is reproduced at the input of the voltage divider VD, which is connected to the second input of the comparator Cmp and is compared by the comparator Cmp with the input voltage U_{in}. When $U_{cv} > U_{in}$ there is a logical "1" level at the Cmp output, and "0" at the Cmp output. With a logical "1" at the output of the Cmp comparator, the control unit (which is conventionally not shown in the diagram in Fig. 1) enables switching of pairs of keys SW1, SW2, SW3, SW4. With logical "0" at the Cmp output, switching of key pairs is not allowed and they remain in their previous state.

As a result of switching pairs of keys, the voltage at the VD input (it is a compensating voltage) after the end of the conversion on any c-cycle is:

$$U_{cv_c} = U_{cv_{c-1}} b^{e_1} b^{e_2} b^{e_3} \cdot \ldots \cdot b^{e_{n-1}} b^{e_n} =$$

$$= U_{cv_{c-1}} \cdot \prod_{i=e_1}^{i=e_n} b^i. \qquad (3)$$

The initial value of the compensation voltage on the first conversion cycle is equal to the reference voltage $U_{cv} = U_r$.

In the last incomplete m-cycle of the conversion, when the compensation voltage is equal to the input voltage ($U_{cv} \le U_{in}$), the conversion ends. With:

– compensation voltage is set equal

$$U_{cv} = U_r \cdot \prod_{i=e_1}^{i=e_n} b^{(m-1)\cdot i} \cdot \prod_{i=e_1}^{i=e_n} a_k b^i; \qquad (4)$$

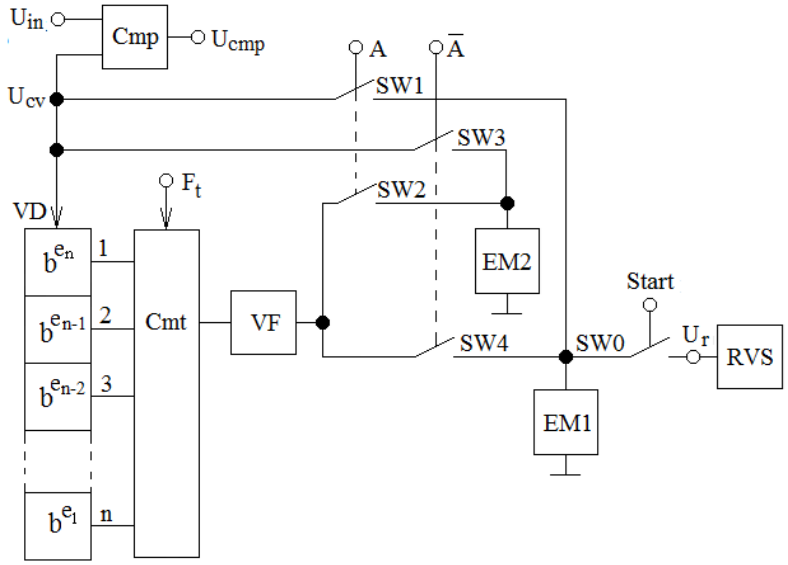

Fig. 1. A simplified structural diagram illustrating the essence of recurrent logarithmic analog-to-digital conversion: It contains comparator Cmp, reference voltage source RVS, voltage divider VD, commutator Cmt, voltage follower VF, 1st and 2nd elements of memory EM1 and EM2, analog switches SW0 – SW4. The figure shows: input voltage U_{in}, *compensation voltage* U_{cv}, *comparator output signal* U_{cmp}; *Start,* A, $\overline{A}$ *are the control signals;* $b^{e_n} \div b^{e_1}$ *are the transfer coefficients of the VD on the outputs* $1 \div n$.

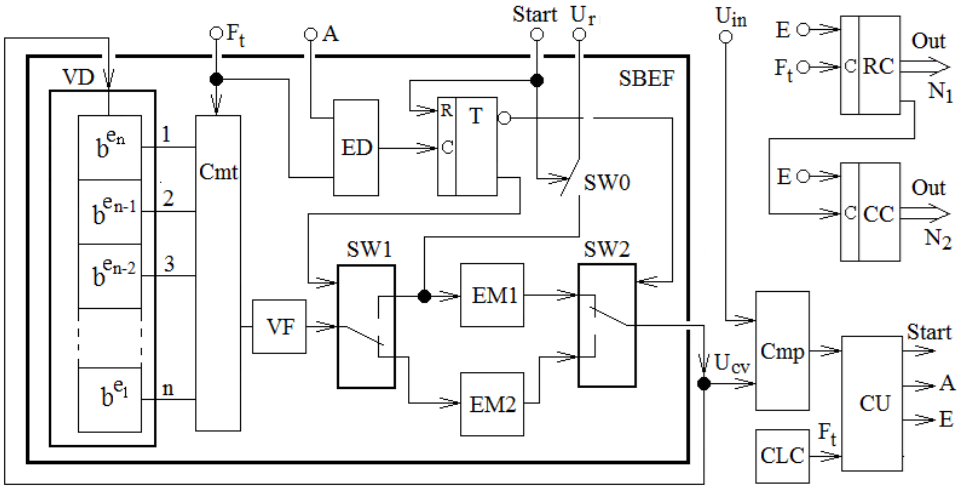

Fig. 2. Generalized structural diagram of recurrent LACP: control unit CU, clock CLC, remainder counter RC, cycle counter CC, scaling block of exponential function SBEF, element of delay ED, trigger T. The figure shows reference voltage U_r, *clock frequency* F_t, *and lower and higher bits respectively* N_1; N_2 *of the source code.*

– the source code of LADC depends on the results of the comparison in each cycle and acquires a value:

$$N = (m-1)\cdot\sum_{i=1}^{n} e^i + \sum_{i=1}^{n} a_k \cdot e^i \qquad (5)$$

and is proportional to the logarithm of the ratio of the input signal to the reference signal;

– the conversion error does not exceed:

$$\delta = \frac{1-b}{b}\cdot 100\%, \qquad (6)$$

here, $a_k = 1$ when the comparison result of the comparator on the i-clock in the m-cycle is equal to logical "1"; $a_k = 0$ when the result of the comparison of the comparator on the i-clock in the m-cycle is equal to logical "0".

The conversion time of the recurrent LADC depends on the repetition period of the clock pulses, the number of conversion cycles, and the clocks in the cycle:

$$t_c \le \left[(m-1)\cdot n + k\right]\cdot T_t, \qquad (7)$$

here T_t is the repetition period of clock pulses, and k is the number of cycles in the last (incomplete) cycle of conversion.

The generalized structural diagram of the recurrent LADC (Fig. 2).

Let's pay attention to the practical implementation of some basic functional nodes of the recurrent LADC: 1) as a counter of the remaining RC, it is advisable to use the standard register of successive approximations (SAR); 2) it is convenient to perform the VD voltage divider based on an adjustable scaling converter with digital switching of transmission coefficients; 3) it is sufficient to use precision capacitors as elements of analog memory EM1 and EM2.

The compensation voltage is reproduced at the output of the SBEF, which is combined with the input of the voltage divider VD and the second input of the comparator Cmp. The CU control unit produces control signals A, E, and Start.

The operation of the generalized structural diagram of the recurrent LADC fig. 2 is clear from the above. We note only the following. If there was a logical "1" at the output of the comparator Cmp, then the CU control unit issues a signal A, which opens the coincidence element ED and the clock pulse passes through the ED and switches the trigger T. If in some cycle the output of Cmp was a logical "0", then the block CU control does not allow signal A to pass, as a result of which a logical "0" will occur at the output of the matching element ED. At the same time, trigger T does not trigger and the state of switches SW1 and SW2 does not change.

According to the "Start" signal, the RC and CC counters, the trigger T are set to zero, and the key SW0 is turned on, through which the reference voltage U_r is entered into the memory element EM1. Through EM2 turned on in the upper position, the voltage from EM1 enters the input of the voltage divider VD, from the first output of which through Cmp, VF, and the switch SW1 is recorded in EM2. After the end of the "Start" signal, the conversion begins as described above.

Recurrent LADCs with a constant base of the logarithm

In the recurrent logarithmic analog-digital conversion with a constant in the process of transformation, the base of the logarithm by dividing the reference voltage (U_r) reproduces a series of reference voltages $U_1 \div U_n$ from which any two adjacent voltage levels differ by the base of the logarithm times:

$$U_1 = \zeta^n U_r;\ U_2 = \zeta^{n-1} U_r;\ U_3 = \zeta^{n-2} U_r;$$
$$U_{n-1} = \zeta^2 U_r \quad \text{i} \quad U_n = \zeta U_r, \qquad (8)$$

here ζ is the base of the logarithm; ζ^n – ζ^1 are the transmission coefficients of the voltage divider VD on outputs 1 – n, which correspond to the coefficients $b^{e_n} \div b^{e_1}$ in Fig. 2.

The process of transformation into the recurrent LADC with a constant base of the logarithm proceeds according to the general principle of action described above. Let's clarify only the following. If there was a logical "1" at the output of the comparator Cmp, then the CU control unit issues signal A, which opens the ED coincidence element and the clock pulse passes through the ED and switches the trigger T. If there was a logical "0" at the output of Cmp in some cycle, then the CU control unit does not allow the passage of signal A, as a result of which a logical "0" will occur at the output of the coincidence element ED. At the same time, trigger T does not trigger and the state of switches SW1 and SW2 does not change.

During the operation of the "Start" signal, the voltage level is set on the element EM2:

$$U_1 = U_r \zeta^n.$$

At the end of the Start signal, the compensation voltage U_{cv} changes with each clock on each conversion cycle as follows.

1. The first conversion cycle. The compensating voltage is set as equal to:

$$U_{cv_1} = U_r \zeta^n \zeta^{n-1} \zeta^{n-2} \cdot \ldots \cdot \zeta^3 \zeta^2 \zeta^1 = U_r \cdot \prod_{i=1}^{i=n} \zeta^i.$$

2. The second conversion cycle. The compensating voltage obtained after the end of the conversion in the first cycle is applied to the input of the VD. After the end of the second cycle, the compensation voltage becomes significant

$$U_{cv_2} = U_{cv_1} \zeta^n \zeta^{n-1} \zeta^{n-2} \cdot \ldots \cdot \zeta^3 \zeta^2 \zeta^1 = U_r \cdot \prod_{i=1}^{i=n} \zeta^{2i}$$

etc.

m-1. In the penultimate m-1 conversion cycle, the compensation voltage is equal to:

$$U_{cv_{m-1}} = U_r \cdot \prod_{i=1}^{i=n} \zeta^{(m-1)\cdot i}.$$

m. In the last incomplete m-cycle of the transformation, when $U_{cv} \le U_{in}$, the transformation ends. With:

– compensation voltage is set equal to:

$$U_{cv} = U_m \cdot \prod_{i=1}^{i=k} \zeta^i = U_r \cdot \prod_{i=1}^{i=n} \zeta^{m\cdot i} \cdot \prod_{i=1}^{i=k} \zeta^i; \qquad (9)$$

– the source code of the recurrent LADC depends on the results of the comparison in each cycle and acquires a value:

$$N = (m-1) \cdot \sum_{i=1}^{n} e^i + \sum_{i=1}^{n} a_k \cdot e^i; \qquad (10)$$

– the conversion error does not exceed [5]:

$$\delta = \frac{1-\zeta}{\zeta} \cdot 100\%. \qquad (11)$$

The conversion time of a recurrent LADC with a constant base is determined by (7).

Recurrent LADCs with a variable base of the logarithm

A feature of recurrent LADCs with a variable logarithm base in the transformation process is the reproduction of a series of reference voltages $U_1 \div U_n$ by dividing the reference voltage U_r, and it is convenient to change the logarithm base according to the binary law:

$$U_1 = \zeta^{\frac{N_z}{2^1}} U_r;\ U_2 = \zeta^{\frac{N_z}{2^2}} U_r;\ U_3 = \zeta^{\frac{N_z}{2^3}} U_r;$$

$$U_{n-1} = \zeta^{\frac{N_z}{2^{n-1}}} U_r \quad \text{i} \quad U_n = \zeta^{\frac{N_z}{2^n}} U_r, \qquad (12)$$

here $\zeta^{\frac{N_z}{2^1}} \div \zeta^{\frac{N_z}{2^n}}$ are the transmission coefficients of the voltage divider VD on outputs 1 – n, which correspond to the coefficients $b^{e_n} \div b^{e_1}$ in Fig. 2; N_z is the nominal value of the LADC source code, determined by the formula [5]:

$$N_z = \frac{1}{\log \zeta} \cdot \log \frac{U_{in}}{U_r}. \qquad (13)$$

The process of conversion to the recurrent LADC with a variable base of the logarithm proceeds cyclically, similar to the one described above for the recurrent LADC with a constant base. During the operation of the "Start" signal, the recurrent LADC is set to its initial position and the voltage level is recorded on the element EM2:

$$U_1 = U_r \zeta^{\frac{N_z}{2^1}}.$$

At the end of the Start signal, the compensation voltage U_{cv} changes with each clock in each conversion cycle as follows.

1. The first conversion cycle.

The voltage at the output of the BFPF after the initial setting is equal to the reference voltage. Therefore, CU generates signal A, as a result of which the first impulse of CLC after the end of the start switches Cmp to the second output of VD and through ED flips the trigger T. Signals from the outputs of T switch switches SW1, SW2, connecting the input EM1 to the output Cmp and the output EM2 to the output SBEF. Comparator Cmp compares the output voltage of the SBEF U_{cv_1} with the input voltage U_{in} and the result of the comparison is entered in the result register SAR. Thus, in the first step of the transformation, the voltage at the output of the SBEF:

$$U_{cv_1} = U_1 = U_r \zeta^{\frac{N_z}{2^1}},$$

and the voltage on EM1 becomes equal to:

$$U_{cv_2} = U_{cv_1} \zeta^{\frac{N_z}{2^2}} = U_r \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}}.$$

For the 2ond measure, the above is repeated. If the result of the comparison U_{cv_2} with U_{in} was a logical "1", then it is entered in the next bit of SAR, and the flip-flop T is switched. As a result, through SW2, the output of EM1 is connected to the VD input, the voltage on which becomes:

$$U_{cv_2} = U_r \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}},$$

and the voltage at the output EM2, connected through SW1 to the 3rd VD output, is equal to:

$$U_{cv_3} = U_r \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}} \zeta^{\frac{N_z}{2^3}}.$$

In the following measures, the transformation takes place similarly. In the last n-clock of the first cycle, the voltage at the output of the SBEF becomes equal to:

$$U_{cv_3} = U_r \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}} \zeta^{\frac{N_z}{2^3}}.$$

After the n-th clock pulse in the first conversion cycle, the CU control unit writes a logical "1" to the counter CC and sets Cmp and the trigger T to the initial state.

2. The second conversion cycle.

In the 2nd conversion cycle, which begins with the n+1 pulse of the CLC, the processes proceed similarly to the 1st cycle. After the end of the 2nd cycle, the voltage at the output of the SBEF is:

$$U_{2n+1} = U_r \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}} \zeta^{\frac{N_z}{2^3}} \cdot \ldots \cdot \zeta^{\frac{N_z}{2^n}} \zeta^{\frac{N_z}{2^{n+1}}} \zeta^{\frac{N_z}{2^{n+2}}} \zeta^{\frac{N_z}{2^{n+3}}} \cdot \ldots \cdot \zeta^{\frac{N_z}{2^{2n}}}.$$

After the end of the last (2n) CLC pulse, a logical "1" is entered into the resulting counter RC, registering "2" conversion cycles.

In subsequent conversion cycles, the processes proceed similarly.

M. The last m-cycle of the transformation.

In the last m-cycle of the conversion, the voltage at the output of the SBEF is equal

$$U_{cv} = U_r \cdot \prod_{k=1}^{m} \prod_{i=1}^{n} \zeta^{a_i \cdot \frac{N_z}{2^{(k-1)n+i}}}. \qquad (14)$$

If on some cycle, for example (m-1)n+2, in the last m-cycle of the conversion, the result of the comparison by the Cmp comparator was a logical "0", then zero will be written in the corresponding bit of the output code of the register SAR, and in the compensation voltage at the output of the SBEF there is no voltage component $\zeta^{\frac{N_z}{2^{(m-1)n+2}}}$ corresponding to this discharge:

$$U_{mn+1} = U_o \zeta^{\frac{N_z}{2^1}} \zeta^{\frac{N_z}{2^2}} \zeta^{\frac{N_z}{2^3}} \cdot \ldots \cdot$$
$$\cdot \zeta^{\frac{N_z}{2^n}} \zeta^{\frac{N_z}{2^{n+1}}} \zeta^{\frac{N_z}{2^{n+2}}} \zeta^{\frac{N_z}{2^{n+3}}} \cdot \ldots \cdot \zeta^{\frac{N_z}{2^{2n}}} \cdot \ldots \cdot$$
$$\cdot \zeta^{\frac{N_z}{2^{(m-1)n+1}}} \zeta^{\frac{N_z}{2^{(m-1)n+3}}} \cdot \ldots \cdot \zeta^{\frac{N_z}{2^{mn}}}.$$

The last $m \cdot n$ – the CLC pulse records the comparison result from the Cmp comparator output into the SAR result register. After the conversion is completed, the upper (N_2) and lower (N_1) digits of the

source code are recorded in the counter CC and the register SAR, respectively. The source code of the variable-base recurrent LADC is:

$$N = N_2 + N_1 = \sum_{k=1}^{m}\sum_{i=1}^{n} a_i \cdot \frac{N_z}{2^{(k-1)n+i}}, \quad (15)$$

here $a_i = 1$ when the result of the comparison of the comparator on the i-clock in the k-cycle is equal to the logical "1"; $a_i = 0$ when the result of the comparison of the comparator on the i-clock in the k-cycle is equal to logical "0".

The 1st logical unit at the output of the comparator is entered in the register SAR and indicates that this cycle is the last. The conversion error does not exceed:

$$\delta = \frac{1 - \zeta^{\frac{N_z}{2^n}}}{\zeta^{\frac{N_z}{2^n}}} \cdot 100\%. \quad (16)$$

The time of transformation of recurrent LADCs with a variable base of the logarithm is determined by (7). Recurrent LADCs with a variable base of the logarithm make it possible to obtain a conversion accuracy higher than the resolution of the LADC itself. For this, the number of transformation cycles "m" must be set according to the formula:

$$m = \frac{N_d}{N_z}, \quad (17)$$

here N_d is the nominal value of the code of the desired bit rate (d), $N_d = 2^d$. Recurrent LADCs with a variable base of the logarithm belong to the class of ADCs with a successive approximation, since in each cycle of the conversion the compensation voltage changes by the binary law according to the change of the base of the logarithm. Therefore, their speed is much higher than the speed of recurrent LACPs with a constant base of the logarithm.

The advantage of the proposed recurrent logarithmic analog-to-digital conversion with a variable base of the logarithm consists of the fact that the desired accuracy is provided by a smaller number of sample values. As a result, the implementation is simplified and the cost of recurrent LADCs is reduced.

5. Conclusions

Based on the conducted issue, we conclude the following:

• recurrent LADCs require a smaller number of reference values compared to LADCs with a successive approximation or flesh;

• recurrent LADCs with a variable base of the logarithm are significantly speedy compared to converters with a constant base;

• increasing the number of conversion cycles in recurrent LADCs with a variable base of the logarithm makes it possible to reach an accuracy higher than the nominal value of the source code. For example, in an 8-bit recurrent LADC, an accuracy of 10 binary digits is obtained in 4 conversion cycles;

• increasing the accuracy of recurrent LADCs with a variable base of the logarithm by more than 2-4 binary digits above the nominal value of the source code is impractical due to a significant increase in the conversion time.

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7. Conflict of interests

The authors declare that there is no financial or other possible conflict related to the current paper.

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