COMPUTATIONAL PROBLEMS OF ELECTRICAL ENGINEERING

**Vol. 12, No. 1, 2022**

# BUCK CONVERTER WITH MAGNETIC-COUPLED INDUCTORS FOR POWER FACTOR CORRECTOR

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https://doi.org/

**Abstract:** The step-down dc-to-dc converter for application in power factor corrector is proposed and analysed in this paper. Unlike a conventional buck converter containing a single inductor and output capacitor, the proposed converter uses two magnetic-coupled inductors and two output capacitors connected in series. The output voltage of such a coupled inductor buck converter is equal to the sum of voltages of these capacitors. The direct interaction of the input voltage occurs only with a part of the output voltage. This allows increasing a conduction angle in the power factor corrector (PFC) on the basis of the proposed converter and, as a result, reducing the total harmonic distortions and increasing a power factor to satisfy current standard requirements. A detailed analysis of the operation of the proposed converter is presented. The reliability of the analysis is confirmed by a small discrepancy between the results of calculation, modeling and experiment.

**Key words:** Buck converter, discontinuous current mode, magnetic-coupled inductor, power factor corrector.

## 1. Introduction

AC-TO-DC converters play the role of power interfaces whose main task is a high-performance conversion of electrical energy of a universal line into energy required for normal operation of dc loads. The harmonic content of the current absorbed from the line and power factor (PF) are regulated by the relevant standards, such as the European standard EN6100-2-3, Energy Star®, etc. To comply with the requirements of the standards, a power factor corrector is included into ac-to-dc converter structure, providing a virtual zero phase shift between the line voltage and current and low level of its current harmonics.

The most popular PFC topology is based on the topology of a boost converter [1] – [4], which provides the unity PF, input current filtering, simplicity, etc. However, despite the widespread applications of the boost converter in the PFC, it has some limitations and drawbacks that worsen its effectiveness in some cases. The high output voltage of the boost converter has a detrimental effect on the switching losses and the higher level of common-mode electromagnetic compatibility noise and determines the need for electronic components with high operating voltages. According to higher values of MOSFET resistances in an on-state, conductive losses increase especially in the PFC with a universal input (90-264 V) when working at of 100-V line. In this case, increased current of boost PFC front end reduces efficiency by 1% -3% compared to that at 220-V (or 230-V) line [5]. In addition, in the case of low-voltage loads (computer, network, telecommunication equipment, etc.), when using such a PFC, it is necessary to have an intermediate step-down conversion that worsens the total efficiency and needs increased requirements for an isolation transformer. With a sudden shutdown of load, the output voltage of boost converter increases uncontrollably.

At lower power levels (below 300-350 W), the drawbacks of the universal-line boost PFC front-end can be overcome by using the PFC front end with buck topology [5]. Buck converter carries out direct conversion of higher voltage to low-level voltage and maintains a high efficiency across the entire line range. Lower output voltage causes a lower level of common mode interference, increases the reliability of the converter and gives the ability to use lower voltage-rated semiconductor devices with better figures of merit.

In [6, 7] the advantages and disadvantages of the buck converter in the PFC front end are analyzed in detail and peculiarities of its practical implementation in the PFC have been developed. In [8] the buck converter has been successfully applied in low cost single-stage high-power-factor electronic ballast of discharge light sources.

The buck converter has a drawback due to the dead zones around zero crossing of line voltage, which is resulted in some current distortion [8]. PF of the buck PFC converter, when operating in discontinuous conduction mode (DCM), is closer to unit if its output voltage is much lower than the amplitude of the line voltage. Fig. 1 shows the waveforms of the input voltage $v_g(t)$, output voltage $V_0$ and input current $i_g(t)$ of the conventional buck PFC converter in DCM. It can be seen

from Fig. 1 that an input current form is the closer to the sinusoidal the closer to $\pi$ is a conduction angle $\theta$. $V_0$ directly interacts with the line voltage and determines the conduction angle:

$$\theta = 2\arccos\frac{V_0}{V_{gm}}, \quad (1)$$

where $V_{gm}$ is a line voltage amplitude.

The analysis of the harmonic content of the input current carried out in [9] shows that the minimum value of the conduction angle $\theta$ which still satisfies the requirements of the European standard IEC-1000-3-2 is about 130° in the absence of a phase shift between the line voltage and current. In this case, the PF of 0.96 and total harmonic distortion (THD) of 29% are obtained. With such a conduction angle, the maximum output voltage of the buck-PFC will be limited to the value of about 130 V at the nominal voltage of the 220-V line. Thus, the limited value of $V_0$ along with the limit value of PF=0.96 constricts the application area of buck converter as a basis for constructing the PFC unit.

Some of improved buck PFC converters were proposed in [10], [11]. They eliminate the undesired dead zones occurred in the conventional buck PFC converter. When the input voltage is lower than the output voltage, one converter operates in buck–boost mode [10], the other operates in flyback mode [11]. However, these converters are complicated and need auxiliary switch circuits.

Therefore, in order to expand the application area of the buck PFC converter, the buck converter modification is proposed in this paper by introducing a coupled inductor, additional output capacitor and diode in the conventional buck converter which widens the conduction angle $\theta$.

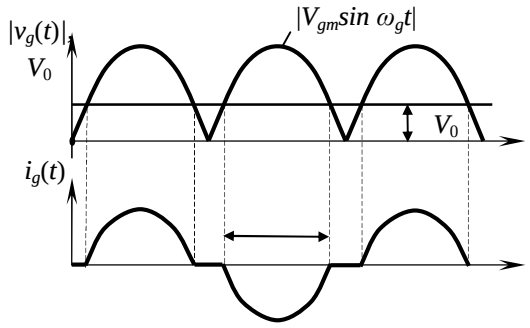



*Fig.1. Waveforms of input voltage $v_g(t)$, output voltage $V_0$ and input current $i_g(t)$ of buck converter PFC in DCM.*

The goal of this work is to develop a buck-type converter with magnetic-coupled inductor for PFC applications which being compared to conventional buck converter allows the increase in the PF at a given output voltage or the increase in the maximum value of the output voltage of the PFC, ensuring the fulfilment of the requirements of standards for the harmonic content of the line current.

2. Operating principle and analysis of coupled inductor buck converter

The topology of the proposed coupled inductor buck converter (CIBC) is similar to the topology of multiple output DC-DC buck converters [12]. The difference consists in the fact that two individual outputs of the converter are connected in series and an obtained common output is connected to the load. The circuit diagram of the CIBC is shown in Fig. 2. Fig. 3 illustrates the operating waveforms of the CIBC. The CIBC consists of a transistor switch $Q_1$, magnetic-coupled inductances $L_1$, $L_2$, diodes $SD_1$, $SD_2$, capacitors $C_1$, $C_2$ and load resistance $R$. A driver circuit controls on/off state of transistor $Q1$. The CIBC operates in DCM.

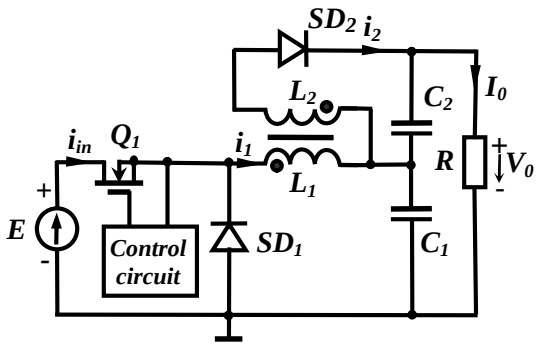



*Fig. 2. Circuit diagram of CIBC*

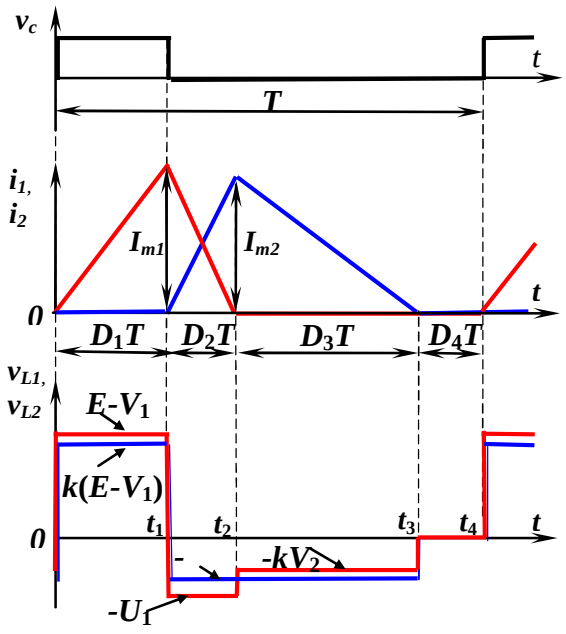



*Fig. 3. Operating waveforms of CIBC*

The output voltage $V_0$ of the CIBC is equal to the sum of voltages $V_1$ and $V_2$ of capacitors $C_1$ and $C_2$ respectively. Since the voltage $V_1$ directly interacts with the line voltage and $V_1$ is less than the output voltage $V_0$, the conduction angle (1) is closer to $\pi$ than in the conventional buck converter with the same output voltage $V_0$. This results in reducing the THD and increasing the PF which better meet the standard requirements or provides a higher PFC output voltage with the same THD and PF.

The following circuit analysis is performed for the steady-state mode. In order to simplify the analysis, the following assumptions are made: all components are ideal, voltages $V_1$ and $V_2$ of capacitors $C_1$ and $C_2$ are constant with a negligible ac ripple; switching frequency is constant.

Each switching period $T$ consists of four time intervals $D_1T$, $D_2T$, $D_3T$ and $D_4T$ that correspond to four operation modes (Fig. 3), where $D_1$, $D_2$, $D_3$ and $D_4$ are duty ratios for the corresponding mode. The duty ratio $D_1$ determines the duration of the on-state of the transistor $Q_1$ and is the control parameter of the CIBC.

**Mode 1 (0-$t_1$):** the transistor $Q_1$ is in a conducting state and the current $i_1$ of inductance $L_1$ increases linearly from zero with the slope determined by the difference between input voltage $E$ and voltage $V_1$ of the capacitor $C_1$. During this interval, the inductance $L_1$ stores energy and its current $i_1$ charges the capacitor $C_1$ maintaining the load current $I_0$. Diodes $SD_1$ and $SD_2$ are in open states and the current $i_2$ of inductor $L_2$ is equal to zero. Voltages $v_{L1}$, $v_{L2}$ and currents $i_1$, $i_2$ of inductors $L_1$ and $L_2$ are respectively equal to:

$$v_{L1} = E - V_1, \tag{2}$$

$$v_{L2} = M\frac{di_1}{dt} = k\left(E - V_1\right), \tag{3}$$

$$i_1 = \frac{E - V_1}{L_1}t, \tag{4}$$

$$i_2 = 0, \tag{5}$$

where $M$ is the mutual inductance and $k$ is the coupling coefficient.

At the end of mode 2, current $i_1$ reaches its maximum $I_{m1}$:

$$I_{m1} = \frac{E - V_1}{L_1}D_1T. \tag{6}$$

Mode 1 ends when the transistor $Q_1$ is turned off at $t_1$.

**Mode 2 ($t_1$-$t_2$):** the transistor $Q_1$ is in the open state and the diodes $SD_1$ and $SD_2$ are in the closed state. The inductance $L_1$ releases energy accumulated in the mode 2 to the capacitor $C_1$ and through the inductance $L_2$ to the capacitor $C_2$ and the load. The inductance current $i_1$ decreases linearly from the maximum value (6) to zero flowing through the diode $SD_1$ and the capacitor $C_1$. The inductance current $i_2$ increases from zero to its maximum value $I_{m2}$ flowing through the diode $SD_2$ and the capacitor $C_2$. Both currents recharge capacitors $C_1$ and $C_2$ respectively, and support the load current $I_0$. The voltages applied accross inductors $L_1$ and $L_2$ are equal to $v_{L1} = -V_1$ and $v_{L2} = -V_2$, respectively. Mode 2 ends at the moment when the current $i_1$ reaches zero.

To determine the duty ratio $D_2$ as a function of $D_1$, we use the equivalent circuit CIBC in mode 2 (Fig. 4). Capacitors $C_1$ and $C_2$ in this circuit are replaced by ideal voltage sources $V_1$ and $V_2$. The change of time $t$ in mode 2 is assumed to range from 0 to $D_2T$. Then the initial current of inductance $L_1$ $i_1(0)=I_{m1}$, and the initial current of the second inductance is equal to zero $i_2(0) = 0$.

According to Kirchhoff's voltage law, we can write down the set of equations:

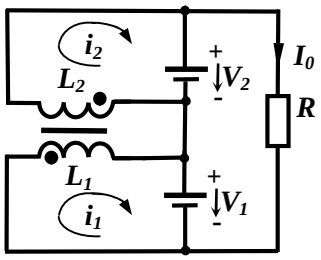



*Fig. 4. CIBC equivalent circuit at mode 2*

$$\begin{cases} L_1\dfrac{di_1}{dt} + M\dfrac{di_2}{dt} + V_1 = 0, \\ M\dfrac{di_1}{dt} + L_2\dfrac{di_2}{dt} + V_2 = 0 \end{cases}. \tag{7}$$

Inductances $L_1$ i $L_2$ are equal $\left(L_1 = L_2 = L\right)$, therefore the expression for mutual inuctance may be written:

$$M = k\sqrt{L_1L_2} = kL. \tag{8}$$

Then, applying the Laplace transformation, the equations (7) can be written in the form:

$$\begin{cases} sL\ I_1(s) + skLI_2(s) = L\ I_1(0) - \dfrac{V_1}{s}, \\ skLI_1(s) + sL\ I_2(s) = kLI_1(0) - \dfrac{V_2}{s}, \end{cases}. \tag{9}$$

where $I_1(s)$, $I_2(s)$ are the Laplace transforms of currents $i_1$, $i_2$ and $I_1(0)= I_{m1}$ is the initial value of the current $i_1$.

The solution of the equations (9) gives the expressions for currents $I_1(s)$ and $I_2(s)$:

$$I_1(s) = \frac{I_1(0)}{s} - \frac{1}{s^2}\frac{V_1 - kV_2}{(1 - k^2)L}, \quad (10)$$

$$I_2(s) = \frac{1}{s^2}\frac{kV_1 - V_2}{(1 - k^2)L}. \quad (11)$$

Hence, taking into account (6), the expressions for the instantaneous currents $i_1$, $i_2$ are obtained:

$$i_1(t) = \frac{E - V_1}{L}D_1T - \frac{V_1 - kV_2}{(1 - k^2)L}t, \quad (12)$$

$$i_2(t) = \frac{kV_1 - V_2}{(1 - k^2)L}t. \quad (13)$$

At the end of mode 2, current $i_1$ becomes zero, so by equating expression (12) to zero (for $t=D_2T$), we can determine the duty ratio $D_2$ as a function of duty ratio $D_1$:

$$D_2 = (1 - k^2)\frac{E - V_1}{V_1 - kV_2}D_1. \quad (14)$$

The current $i_2$ reaches its maximum value $I_{m2}$ at the end of the mode 2. Using (13), (14) and (6), this value $I_{m2}$ is represented by the expression:

$$I_{m2} = \frac{kV_1 - V_2}{V_1 - kV_2}I_{m1}. \quad (15)$$

Let $V_1$ and $V_2$ be written as $V_1 = \alpha V_0$ and $V_2= (1-\alpha)V_0$ respectively, where $0< \alpha <1$. Then (15) may be rewritten as

$$I_{m2} = \frac{a(1+k) - 1}{a(1+k) - k}I_{m1}. \quad (16)$$

The coupling coefficient $k<1$, therefore, the numerator of (16) is less than its denominator and $I_{m2}<I_{m1}$. So the energy transferred by the inductor $L_2$ to the capacitor $C_2$ is less than the energy transferred by the inductor $L_1$ to the capacitor $C_1$. Therefore, the voltage $V_2$ is less than voltage $V_1$: ($V_2< V_1$).

**Mode 3 ($t_2$-$t_3$)**: the transistor $Q_1$ and the diode $SD_1$ are in the open state and the diode $SD_2$ is in the closed state. The inductance $L_2$ releases the energy accumulated in the mode 2 to the capacitor $C_2$ and the load. At the beginning of this mode, the current of the second inductance is equal to its maximum (15). The voltages at the inductors $L_1$ and $L_2$ are equal to $v_{L1} = -kV_2$ and $v_{L2} = -V_2$, respectively. Mode 3 ends at the time when the current $i_2$ reaches zero.

To determine the duty ratio $D_3$ as a function of $D_1$ we can express $I_{m2}$ through the interval $D_3T$, namely:

$$I_{m2} = -\frac{di_2}{dt}D_3T = \frac{V_2}{L}D_3T. \quad (17)$$

Equating (15) and (17) and taking into account (14), we obtain the expression for the duty ratio $D_3$:

$$D_3 = \frac{E - V_1}{V_2}\frac{kV_1 - V_2}{V_1 - kV_2}D_1. \quad (18)$$

**Mode 4 ($t_3$-$t_4$)**: the transistor $Q_1$ and the diodes $SD_1$, $SD_2$ are in the open state. Currents and voltages of both inductors are zero. The capacitors $C_1$ and $C_2$ support the load current $I_0$.

**3. DC transfer function of the converter**

The DC transfer function of the CIBC is considered as a ratio between output voltage and input voltage which depends on the control parameter $D_1$:

$$M = \frac{V_0(D_1)}{E}, \quad (19)$$

where $V_0(D_1) =V_0$ is a function of duty ratio $D_1$ and is equal to:

$$V_0(D_1) = V_1 + V_2. \quad (20)$$

To calculate the transfer function of the converter using time diagrams (Fig. 3), a set of equations for voltages $V_1$ and $V_2$ and for pre-unknown duty ratios $D_2$ and $D_3$ is obtained.

Using volt-second balances at the inductors $L_1$ and $L_2$ in the steady state, the first two equations can be expressed as follows:

$$(E - V_1)D_1 - V_1D_2 - kV_2D_3 = 0, \quad (21)$$

$$k(E - V_1)D_1 - V_2(D_2 + D_3) = 0. \quad (22)$$

The two following equations describe the average values of inductor currents for the switching period. These equations take into account the fact that the average currents of both inductors are equal to the load current of the converter. The average currents of inductances $L_1$, $L_2$ using (6) and (17) respectively are equal to:

$$\frac{E - V_1}{2L}D_1T(D_1 + D_2) = \frac{V_1 + V_2}{R}, \quad (23)$$

$$\frac{V_2}{2L}D_3T(D_2 + D_3) = \frac{V_1 + V_2}{R}. \quad (24)$$

The condition of the operation of the converter in DCM must be fulfilled:

$$D_1 + D_2 + D_3 \le 1. \quad (25)$$

For the convenience of the following design procedure, generalized parameter $Q$ of the CIBC which combines the main parameters of the converter determining its operation (namely, inductance, load resistance, switching period) is introduced:

$$Q = \frac{2L}{RT}. \tag{26}$$

Then the resulting set of equations (21) - (25) takes the form:

$$\begin{cases} (E - V_1)D_1 - V_1D_2 - kV_2D_3 = 0; \\ k(E - V_1)D_1 - V_2D_3 = 0; \\ \dfrac{E - V_1}{Q} D_1(D_1 + D_2) = V_1 + V_2; \\ k(E - V_1)D_1 - V_2(D_2 + D_3) = 0 \\ D_1 + D_2 + D_3 \le 1. \end{cases} \tag{27}$$

Unknowns in (27) are the required voltages $V_1$, $V_2$ and the duty ratios $D_2$, $D_3$ which are interrelated with these voltages. To solve (27), we will consider the following parameters given:

- input voltage $E$,
- duty ratio $D_1$;
- generalized parameter $Q$;
- coupling coefficient $k$.

The solution of the set (27) was found by numerical methods because in analytical form its subsequent interpretation and use is too cumbersome.

The results of calculation taking into account the expressions (19) and (20) are presented in Fig. 5 and Fig. 6. Fig. 5 demonstrates the dependences of the transfer function $M$ on the control parameter $D_1$ for different values of generalized parameter $Q$ at a given coupling coefficient $k$ = 0.95. After considering these dependences, it can be concluded that, for example, the values of the parameter $Q$=0.08 provides a wide range of changes of a transfer function M (from 0 to 0.9) when changing the duty ratio $D_1$ in a wide range from 0 to 0.45. The parameter $Q$ affects the maximum value of the duty ratio $D_1$ at which the converter is still operating in DCM. If $Q$ is about $Q$≈0.12 and more, the converter has a small control range or goes into continuous current mode and loses its properties.

Fig. 6 shows the dependences of voltage ratio $\mathrm{a} = \dfrac{V_1}{V_0}$ on the duty ratio $D_1$ for different values of $Q$ at a given $k$=0.95. The coefficient α shows what part of the output voltage is the voltage $V_1$ which directly interacts with the input voltage $E$. The smaller α is, the larger the conduction angle (1) is, and, therefore, the less distortion introduced by the CIBC PFC.

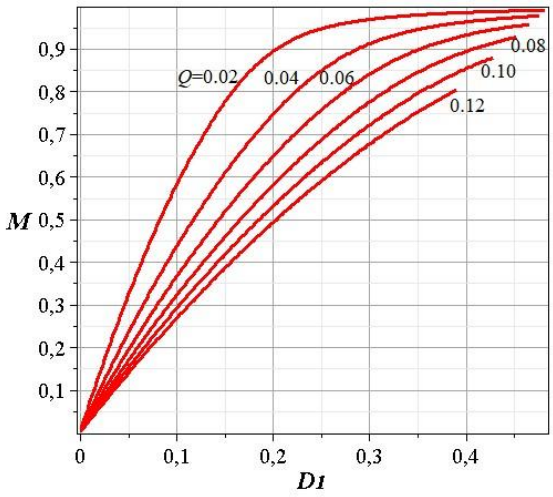



*Fig. 5. Dependences of the transfer function M on the duty ratio $D_1$ for different values of the generalized parameter Q*

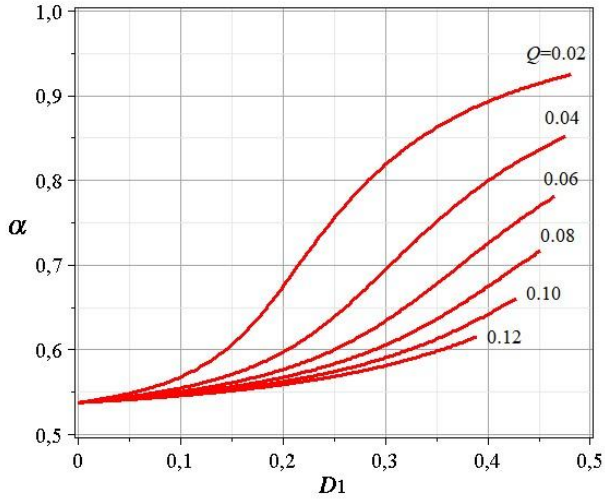



*Fig. 6. Dependences of the voltage ratio $\mathrm{a} = \dfrac{V_1}{V_0}$ on the duty ratio $D_1$ for different values of the generalized parameter Q*

**4. Verification of coupled inductor buck converter**

For verification of proposed CIBC, its simulation, PSIM-model, and experimental prototype were carried out. In order to test the goodness of the proposed CIBC structure, a prototype has been designed according to the following specification:

1) input voltage $E$=30 V;
2) coupling coefficient $k$=0.95;
3) load resistance $R$=150 Ohm;
4) control circuit is realized with the use of the step-down voltage regulator LM2575 with operation frequency $f$=56 kHz.

Using Fig. 5 and Fig.6, generalized parameter $Q$ = 0.08 is chosen which provides a wide range of $M$ (from 0 to 0.9) and small voltage ratio α (from 0.54 to 0.72). From (26), the inductance $L$=107 μH can be calculated.

For duty ratio $D_1$=0.35, Fig. 7 demonstrates the simulation waveforms of inductor voltages $v_{L1}$, $v_{L2}$ and currents $i_1$, $i_2$, capacitor voltages $V_1$, $V_2$ and output voltage $V_0$.

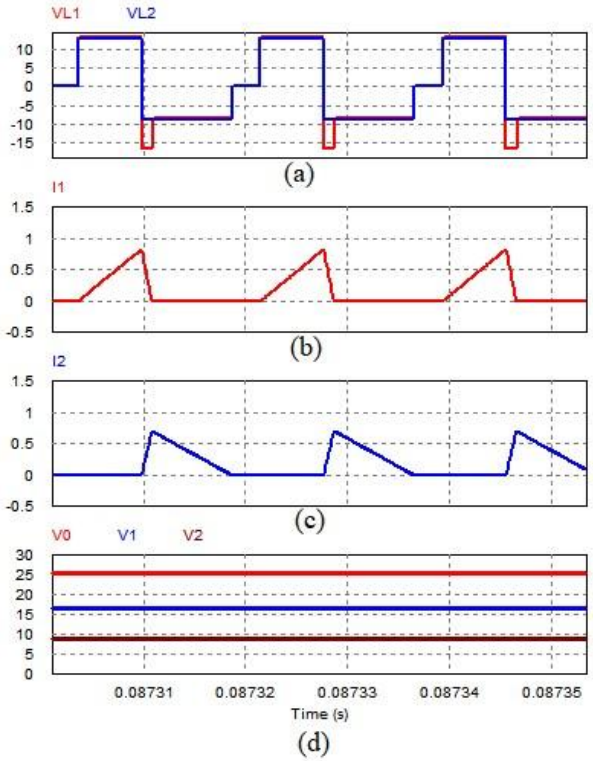
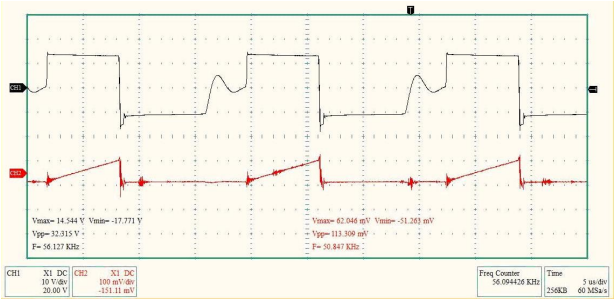



*Fig. 7. Simulation results (for $D_1$=0.35): (a) inductor voltages $v_{L1}$, $v_{L2}$; (b) and (c) inductor currents $i_1$ and $i_2$; (d) output voltage $V_0$ and capacitor voltages $V_1$, $V_2$*

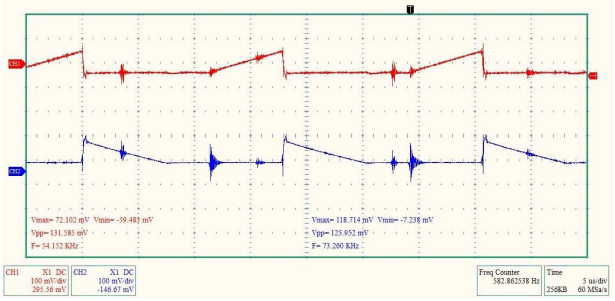
In Fig. 8, the top traces show the experimental curves of voltage $v_{L1}$ and current $i_1$ of the inductor $L_1$ and the bottom traces show the inductor currents $i_1$ and $i_2$. The results of modeling and experiment are well coordinated.

According to the results of the analysis of the CIBC with parameters that correspond to the model and experiment, the calculations of the output voltage $V_0$ for different values of $D_1$ were carried out. For the same values $D_1$, the output voltages of the simulation model and of the prototype were obtained. The results of calculation, modeling and experiment are collected in Table 1. A small discrepancy between these results confirms the adequacy of the performed analysis.

To demonstrate the possibility of using the CIBC in PFC, a comparative simulation of the PFC with the conventional buck converter and the PFC with the proposed CIBC was executed. Each PFC was incorporated into the single-stage electronic ballast structure for two fluorescent lamps Osram L-36W [8] when powered by AC 220 V. The simulation results of input currents for these PFC units are shown in Fig. 9.



*a)*



*b)*

*Fig. 8. Experimental waveforms:*
*(a) voltage and current of inductance $L_1$;*
*(b) currents of inductors $L_1$ and $L_2$.*

*Table 1*

**Dependences of $V_0$ on $D_1$: calculation, modeling and experiment**

| $D_1$ | $V_0$, V for $Q$=0.075 and $k$=0.95 | | |
|---|---|---|---|
| | Calculation | Modeling | Experiment |
| 0.05 | 5.2229 | 5.2218 | 5.2 |
| 0.15 | 14.1398 | 14.1387 | 13.7 |
| 0.25 | 21.0561 | 21.0550 | 20.7 |
| 0.35 | 25.7145 | 25.6594 | 25.2 |
| 0.45 | 27.9945 | 27.8917 | 27.4 |

According to the simulation, the THD of the PFC with the CIBC is near 15%, and its PF is 0.99. Under the same conditions, the PFC with the conventional buck converter [8] shows THD equal to 30% and its PF factor is 0.96.

Thus, the use of the proposed CIBC in the PFC allows reducing the level of the harmonic content of PFC and increasing its power factor.

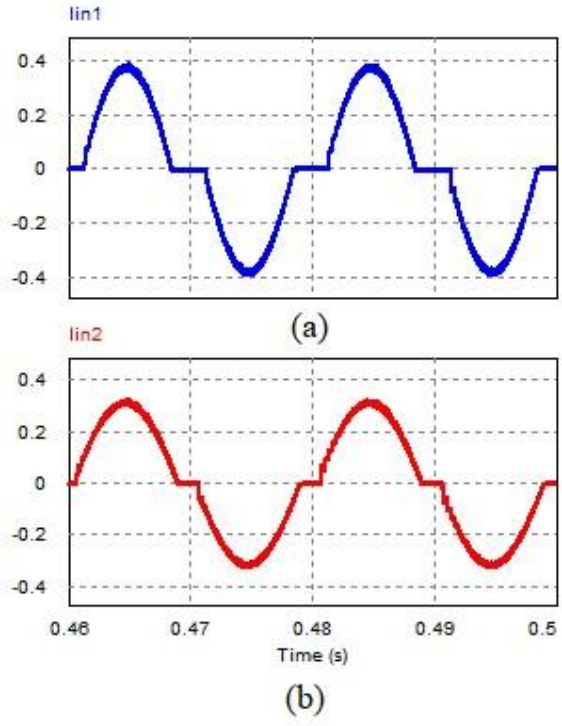



*Fig. 9. Results of PFC input current modeling:*
*(a) with conventional buck converter;*
*(b) with proposed CIBC*

**5. Conclusion**

In this paper, the coupled inductor buck converter designed for use in a power factor corrector is proposed and investigated. The converter operates in discotinuous current mode. The formation of the output voltage in such a converter takes place due to the use of two magnetically coupled inductances and two series-connected capacitors. Due to this, the direct interaction of the input voltage goes on only with a part of the output voltage, which allowes the increase in the conduction angle in the power factor corrector based on the proposed converter and, as a result, reduction in the total harmonic distortions and the increase in the power factor. The results of the analysis of the converter are the basis for its design procedure. Comparative analysis of the calculation, modeling and experiment results demonstrates a high degree of compliance.

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## ЗНИЖУВАЛЬНИЙ ПЕРЕТВОРЮВАЧ НАПРУГИ З МАГНІТНО-ЗВ'ЯЗАНИМИ ІНДУКТИВНОСТЯМИ ДЛЯ КОРЕКТОРА КОЕФІЦІЄНТА ПОТУЖНОСТІ

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Запропоновано та проаналізовано знижувальний перетворювач постійної напруги для застосування в коректорі коефіцієнта потужності. На відміну від традиційного знижувального перетворювача, який містить одну індуктивність та вихідний конденсатор, пропонований перетворювач має дві магнітно-зв'язані індуктивності і два послідовно з'єднані вихідні конденсатори. Вихідна напруга пропонованого знижувального перетворювача дорівнює сумі напруг на цих конденсаторах. Безпосередня взаємодія вхідної напруги здійснюється з напругою одного конденсатора, тобто, лише з частиною вихідної напруги. Це дає змогу збільшити кут провідності в коректорі коефіцієнта потужності на основі запропонованого перетворювача і, як наслідок, зменшити коефіцієнт гармонік та збільшити коефіцієнт потужності, щоб задовольнити вимоги чинних стандартів. Перетворювач працює в режимі переривчастого струму на постійній частоті. Проведено детальний аналіз роботи запропонованого перетворювача. Достовірність аналізу підтверджено малою розбіжністю між результатами розрахунку, моделювання та експерименту.

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*Received: 19.01.2022. Accepted: 30.03.2022*